

Compal Confidential

STORM M/B Schematic

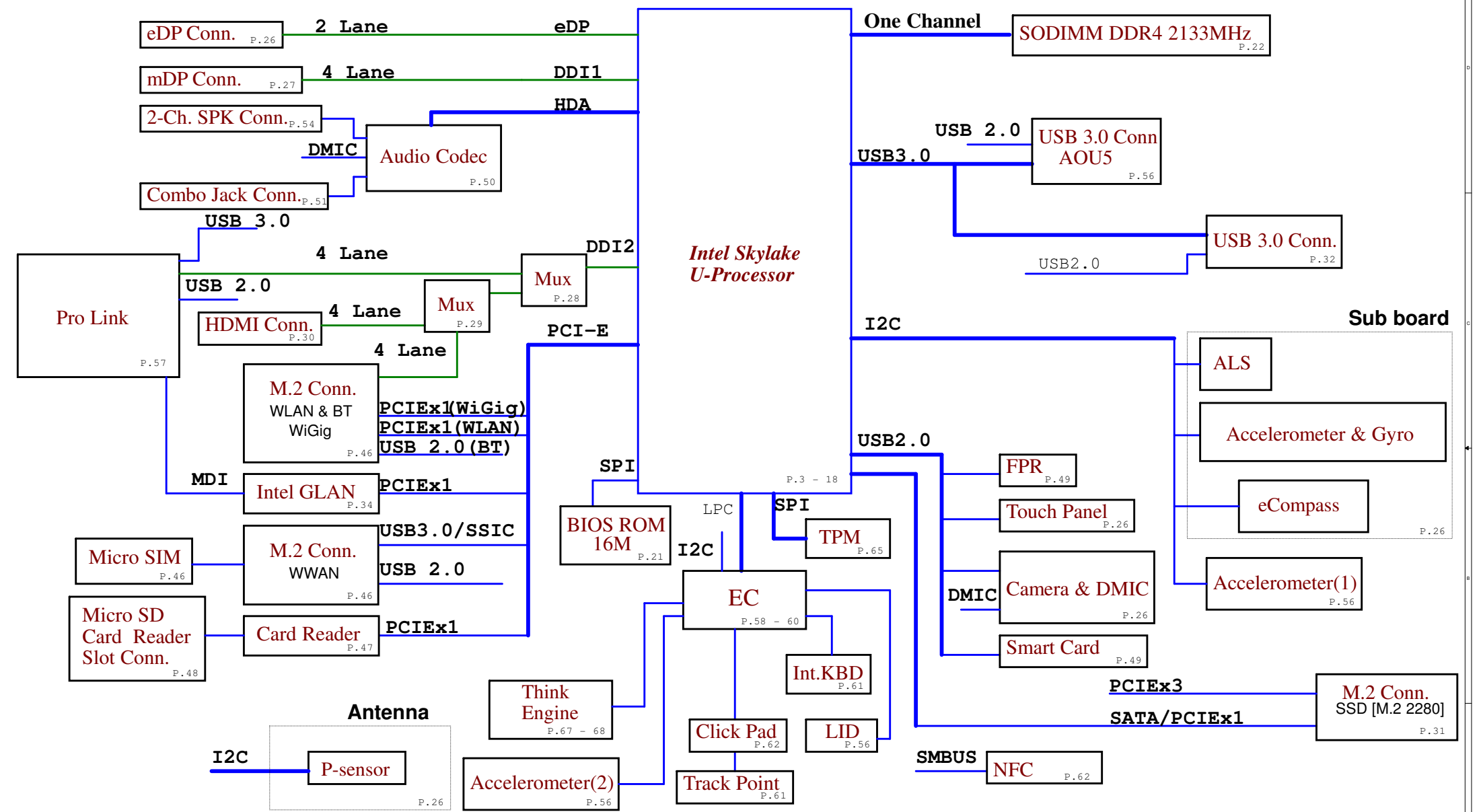
LA-C581P

Rev: 1.0_D

2015.08.13

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	COVER PAGE
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				Custom	LA-C581P
				Date	Thursday, August 13, 2015
				Sheet	1 of 102
				Rev	0.5

STORM Block-Diagram



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	BLOCK DIAGRAM
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Size	Document Number	LA-C581P			Date
Custom	Thursday, August 13, 2015	Sheet	2	of	102

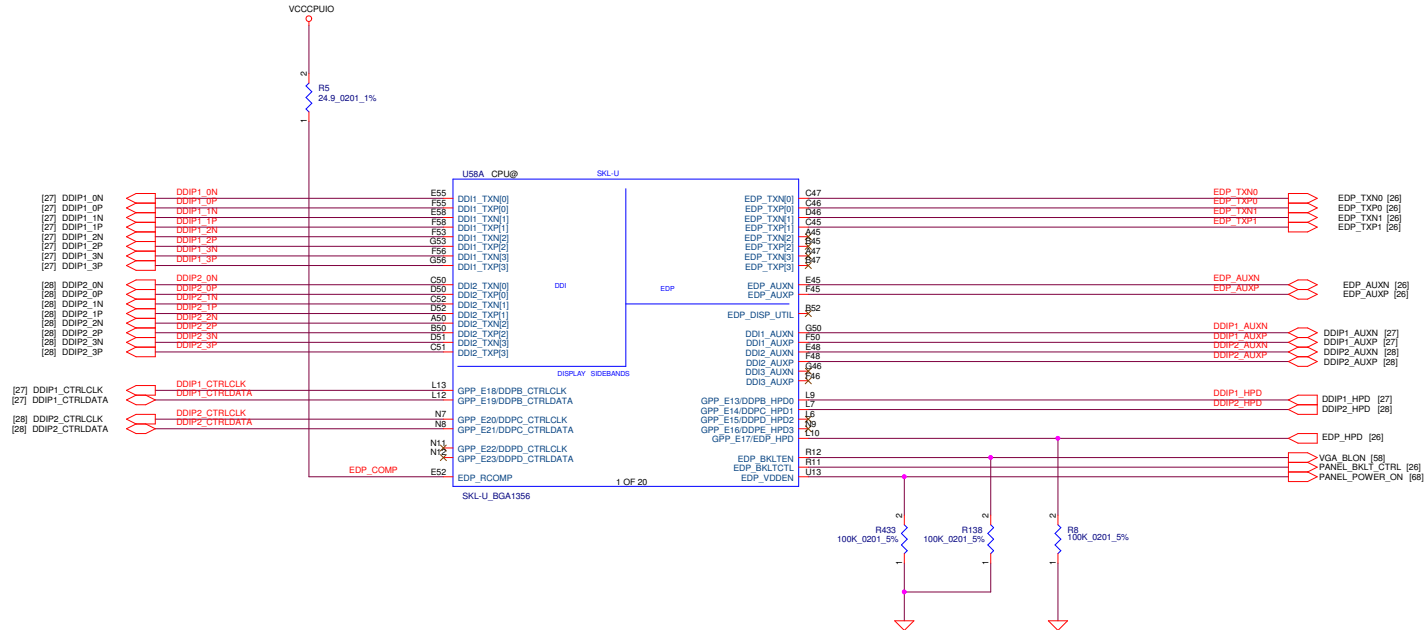
TABLE : Function Strap

DDPB_CTRLDATA

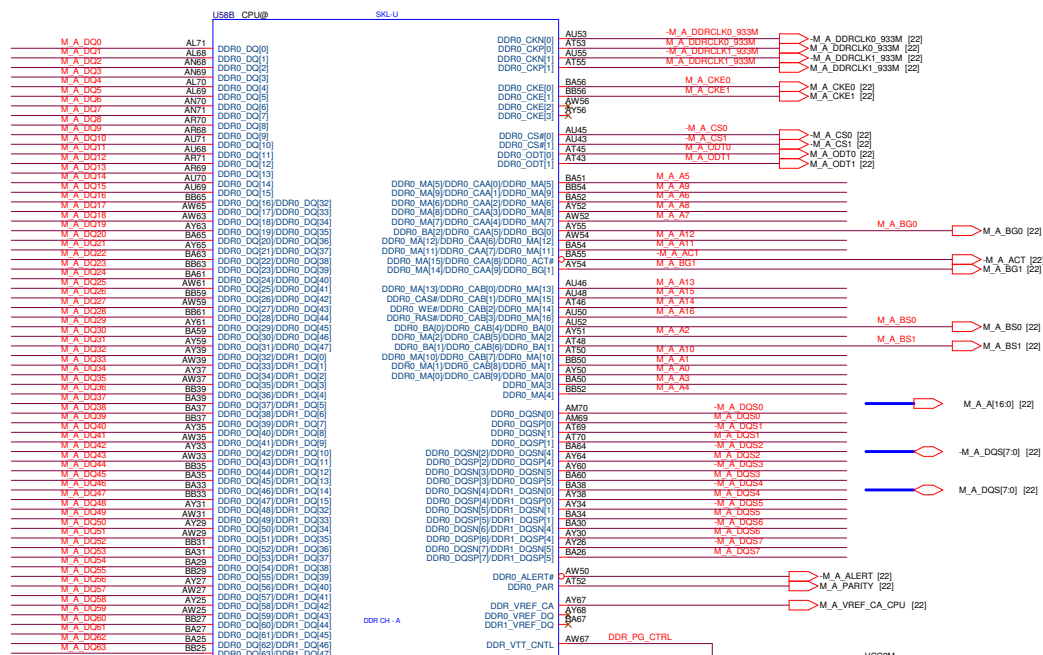
HIGH Port B is detected.
LOW Port B is not detected.

DDPC_CTRLDATA

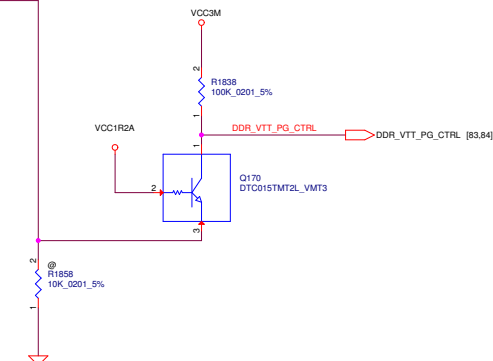
HIGH Port C is detected.
LOW Port C is not detected.



	Pin	Interleave	Non-Interleave
Block 0	AL71	DDRO_DQ[0]	DDRO_DQ[0]
	AL68	DDRO_DQ[1]	DDRO_DQ[1]
	AN68	DDRO_DQ[2]	DDRO_DQ[2]
	AN69	DDRO_DQ[3]	DDRO_DQ[3]
	AL70	DDRO_DQ[4]	DDRO_DQ[4]
	AL69	DDRO_DQ[5]	DDRO_DQ[5]
	AN70	DDRO_DQ[6]	DDRO_DQ[6]
	AN71	DDRO_DQ[7]	DDRO_DQ[7]
	AR68	DDRO_DQ[8]	DDRO_DQ[8]
	AE68	DDRO_DQ[9]	DDRO_DQ[9]
	AU71	DDRO_DQ[10]	DDRO_DQ[10]
	AU68	DDRO_DQ[11]	DDRO_DQ[11]
	AR71	DDRO_DQ[12]	DDRO_DQ[12]
	AR69	DDRO_DQ[13]	DDRO_DQ[13]
AU70	DDRO_DQ[14]	DDRO_DQ[14]	
AU69	DDRO_DQ[15]	DDRO_DQ[15]	
Block 2	BB65	DDRO_DQ[16]	DDRO_DQ[32]
	AW65	DDRO_DQ[17]	DDRO_DQ[33]
	AW63	DDRO_DQ[18]	DDRO_DQ[34]
	AY63	DDRO_DQ[19]	DDRO_DQ[35]
	BA65	DDRO_DQ[20]	DDRO_DQ[36]
	AY65	DDRO_DQ[21]	DDRO_DQ[37]
	BA63	DDRO_DQ[22]	DDRO_DQ[38]
	BB63	DDRO_DQ[23]	DDRO_DQ[39]
	BA61	DDRO_DQ[24]	DDRO_DQ[40]
	AW61	DDRO_DQ[25]	DDRO_DQ[41]
	BB59	DDRO_DQ[26]	DDRO_DQ[42]
	AW59	DDRO_DQ[27]	DDRO_DQ[43]
	BB61	DDRO_DQ[28]	DDRO_DQ[44]
	AY61	DDRO_DQ[29]	DDRO_DQ[45]
BA59	DDRO_DQ[30]	DDRO_DQ[46]	
AY59	DDRO_DQ[31]	DDRO_DQ[47]	
Block 4	AY39	DDRO_DQ[32]	DDRI_DQ[0]
	AW39	DDRO_DQ[33]	DDRI_DQ[1]
	AY37	DDRO_DQ[34]	DDRI_DQ[2]
	AW37	DDRO_DQ[35]	DDRI_DQ[3]
	BB39	DDRO_DQ[36]	DDRI_DQ[4]
	BA39	DDRO_DQ[37]	DDRI_DQ[5]
	BA37	DDRO_DQ[38]	DDRI_DQ[6]
	BB37	DDRO_DQ[39]	DDRI_DQ[7]
	AY35	DDRO_DQ[40]	DDRI_DQ[8]
	AW35	DDRO_DQ[41]	DDRI_DQ[9]
	AY33	DDRO_DQ[42]	DDRI_DQ[10]
	AW33	DDRO_DQ[43]	DDRI_DQ[11]
	BB35	DDRO_DQ[44]	DDRI_DQ[12]
	BA35	DDRO_DQ[45]	DDRI_DQ[13]
BA33	DDRO_DQ[46]	DDRI_DQ[14]	
BB33	DDRO_DQ[47]	DDRI_DQ[15]	
Block 6	AY31	DDRO_DQ[48]	DDRI_DQ[32]
	AW31	DDRO_DQ[49]	DDRI_DQ[33]
	AY29	DDRO_DQ[50]	DDRI_DQ[34]
	AW29	DDRO_DQ[51]	DDRI_DQ[35]
	BB31	DDRO_DQ[52]	DDRI_DQ[36]
	BA31	DDRO_DQ[53]	DDRI_DQ[37]
	BA29	DDRO_DQ[54]	DDRI_DQ[38]
	BB29	DDRO_DQ[55]	DDRI_DQ[39]
	AY27	DDRO_DQ[56]	DDRI_DQ[40]
	AW27	DDRO_DQ[57]	DDRI_DQ[41]
	AY25	DDRO_DQ[58]	DDRI_DQ[42]
	AW25	DDRO_DQ[59]	DDRI_DQ[43]
	BB27	DDRO_DQ[60]	DDRI_DQ[44]
	BA27	DDRO_DQ[61]	DDRI_DQ[45]
BA25	DDRO_DQ[62]	DDRI_DQ[46]	
BB25	DDRO_DQ[63]	DDRI_DQ[47]	



	Pin	Interleave	Non-Interleave
Block 0	AM70 AM69 AT69 AT70	DDRO_DQSN[0] DDRO_DQSP[0] DDRO_DQSN[1] DDRO_DQSP[1]	DDRO_DQSN[0] DDRO_DQSP[0] DDRO_DQSN[1] DDRO_DQSP[1]
Block 2	BA64 AY64 AY60 BA60	DDRO_DQSN[2] DDRO_DQSP[2] DDRO_DQSN[3] DDRO_DQSP[3]	DDRO_DQSN[4] DDRO_DQSP[4] DDRO_DQSN[5] DDRO_DQSP[5]
Block 4	BA38 AY38 AY34 BA34	DDRO_DQSN[4] DDRO_DQSP[4] DDRO_DQSN[5] DDRO_DQSP[5]	DDRI_DQSN[0] DDRI_DQSP[0] DDRI_DQSN[1] DDRI_DQSP[1]
Block 6	BA30 AY30 AY26 BA26	DDRO_DQSN[6] DDRO_DQSP[6] DDRO_DQSN[7] DDRO_DQSP[7]	DDRI_DQSN[4] DDRI_DQSP[4] DDRI_DQSN[5] DDRI_DQSP[5]



Pin	D0R3	LPDDR3	DDR4
BAS1	DDRO_M[A]5	DDRO_CAA[0]	DDRO_M[A]5
BAS2	DDRO_M[A]6	DDRO_CAA[1]	DDRO_M[A]6
AY52	DDRO_M[A]8	DDRO_CAA[3]	DDRO_M[A]8
AW52	DDRO_M[A]7	DDRO_CAA[4]	DDRO_M[A]7
AY55	DDRO_BA[2]	DDRO_CAA[5]	DDRO_BG[0]
AW54	DDRO_M[A]12	DDRO_CAA[6]	DDRO_M[A]12
BAS4	DDRO_M[A]11	DDRO_CAA[7]	DDRO_M[A]11
BAS5	DDRO_M[A]15	DDRO_CAA[8]	DDRO_ACT9
AY54	DDRO_M[A]14	DDRO_CAA[9]	DDRO_BG[1]
AU46	DDRO_M[A]13	DDRO_CAB[0]	DDRO_M[A]13
AU48	DDRO_CAS5	DDRO_CAB[1]	DDRO_M[A]15
AT46	DDRO_W#8	DDRO_CAB[2]	DDRO_M[A]14
AU52	DDRO_BA[0]	DDRO_CAB[3]	DDRO_BA[0]
AY51	DDRO_M[A]2	DDRO_CAB[5]	DDRO_M[A]2
AT48	DDRO_BA[1]	DDRO_CAB[6]	DDRO_BA[1]
AT50	DDRO_M[A]10	DDRO_CAB[7]	DDRO_M[A]10
BBS0	DDRO_M[A]1	DDRO_CAB[8]	DDRO_M[A]1
AY50	DDRO_M[A]0	DDRO_CAB[9]	DDRO_M[A]0
DDRO_M[A]3	DDRO_M[A]3	Not Used	DDRO_M[A]3
DDRO_M[A]4	DDRO_M[A]4	Not Used	DDRO_M[A]4

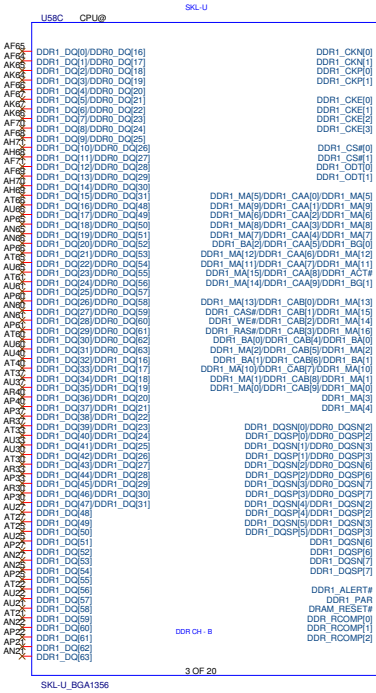
↑
LOGIC

Security Classification		Compal Secret Data		Title	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Compal Electronics, Inc. CPU(2/16) : DDR CHANNEL-A	
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				Date: Thursday, August 13, 2015	Sheet 4 of 102

TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AH70	DDR1_DQ[13]	DDR0_DQ[29]
	AF69	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU30	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

LOGIC



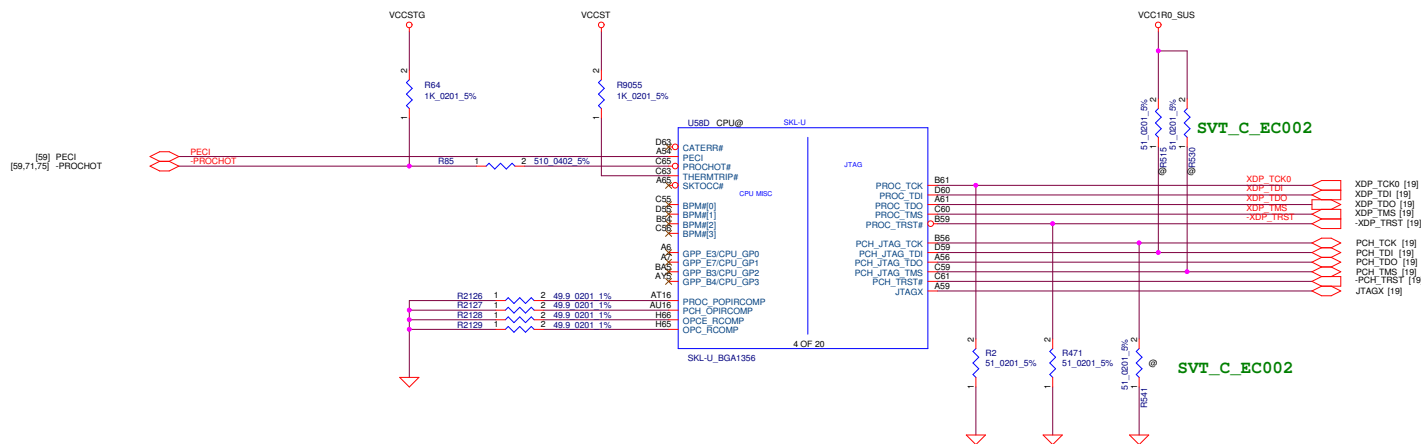
	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AT32	DDR1_DQSP[4]	DDR1_DQSP[2]
	AR32	DDR1_DQSN[5]	DDR1_DQSN[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
Block 7	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

LOGIC

TABLE

Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_BA[0]	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[1]	DDR1_CAB[4]	DDR1_MA[10]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

LOGIC



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Issued Date	2014/11/04	Deciphered Date	2016/12/31
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SPI0_MOSI (Boot Halt)	
HIGH	Disabled (Default)
LOW	Enabled

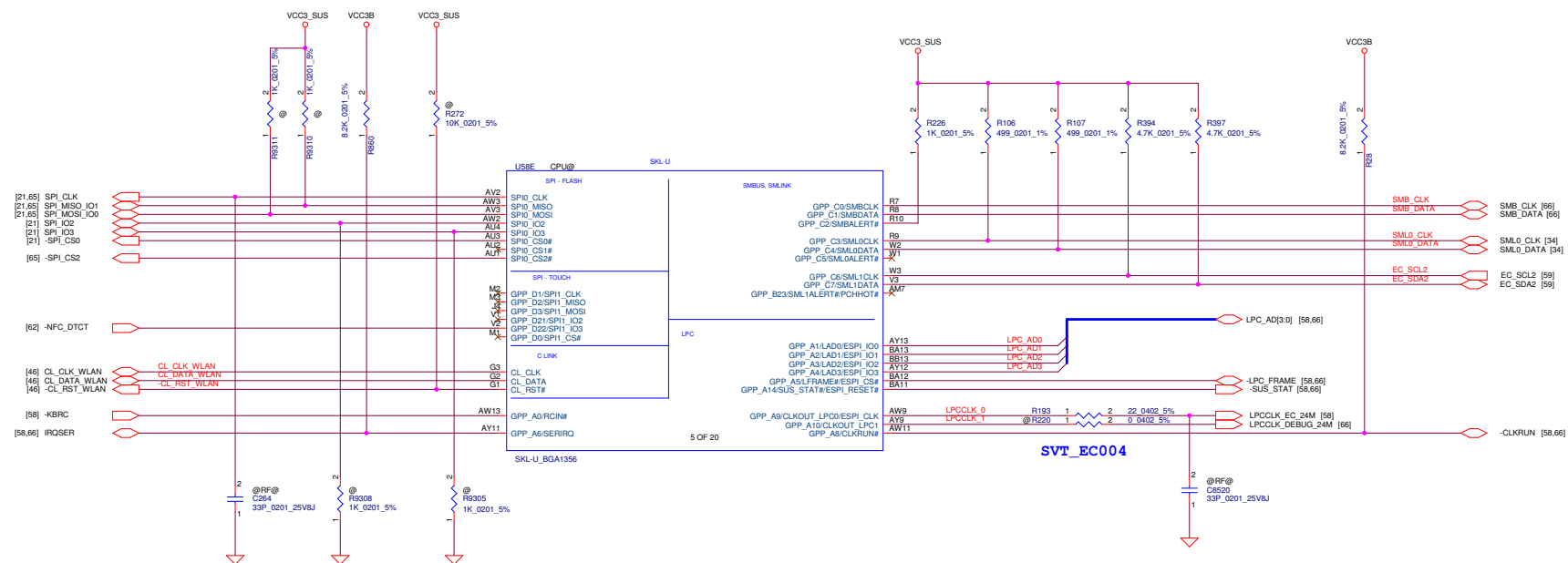
SPI0_MISO (JTAG ODT Diabler)	
HIGH	Enabled (Default)
LOW	Disabled

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

← LOGIC



SPI0_IO2 (Consent Strap)	
HIGH	Enabled (Default)
LOW	Disabled

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled (Default)
LOW	Enabled

Security Classification	Compal Secret Data		Compal Electronics, Inc. CPUS(i16) : LPC/SPI/SMBUS/C-LINK	
Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title CPUS(i16) : LPC/SPI/SMBUS/C-LINK
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			Date Thursday, August 13, 2015	
			Sheet 7 of 102	

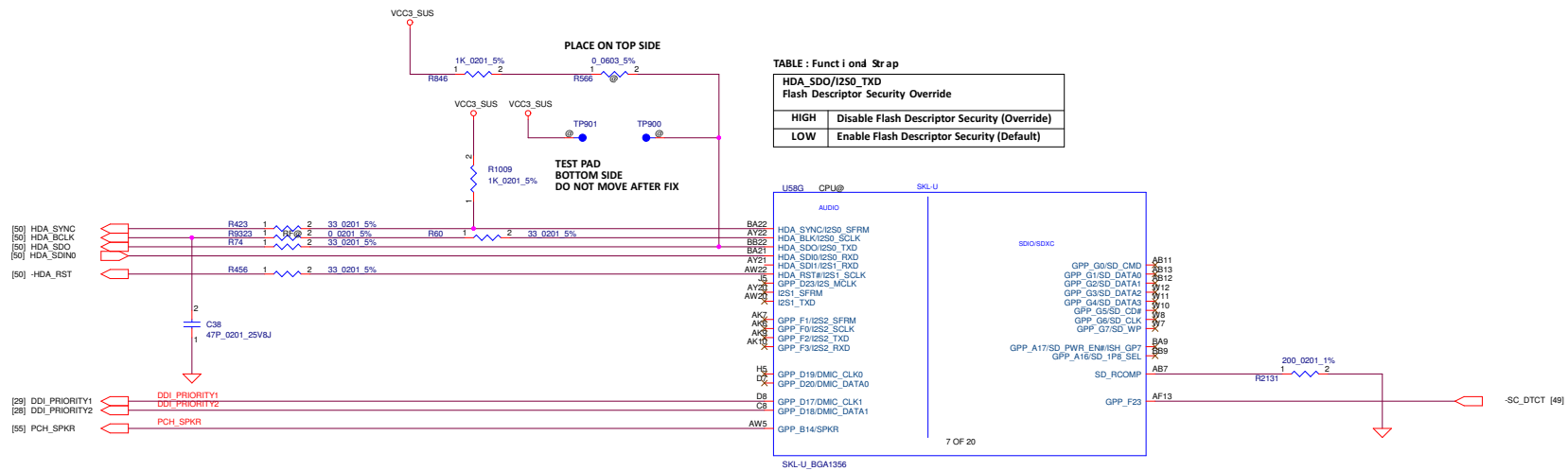


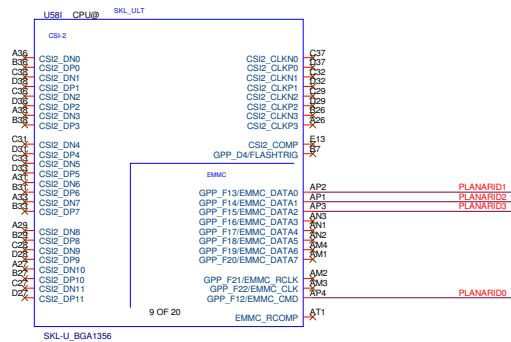
TABLE : Function Strap

HDA_SDO/I2SD_TXD Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

TABLE : Function Strap

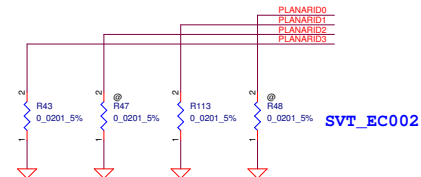
GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" Mode
LOW	Disable "Top Swap" Mode (Default)

← LOGIC



TABLE

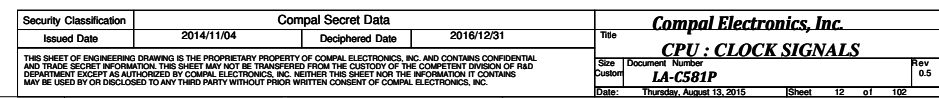
LEVEL	PLANAR ID			
	3	2	1	0
	R43	R47	R113	R48
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

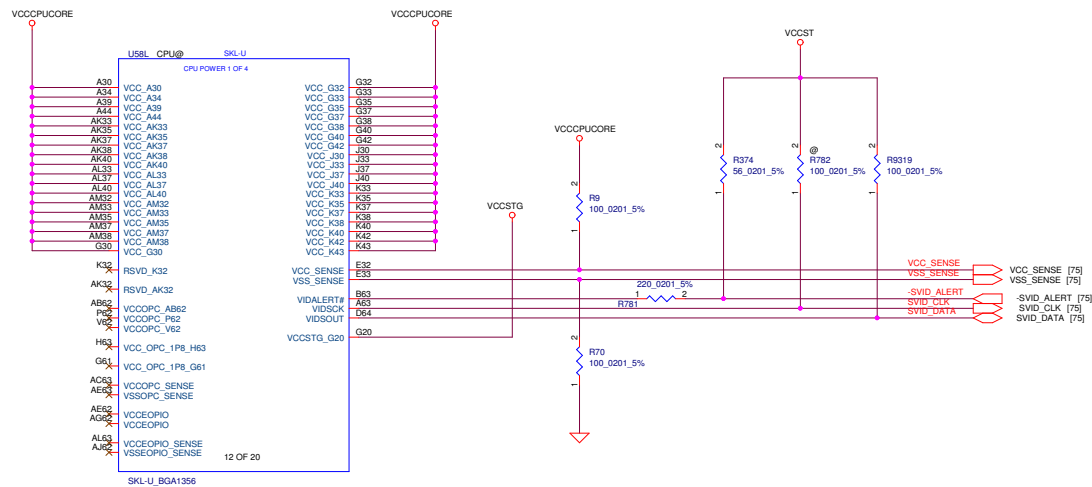


TABLE

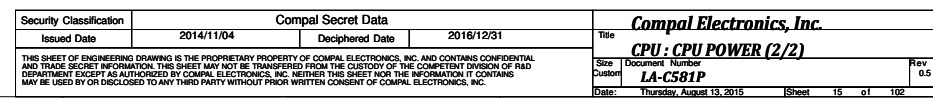
LEVEL	PLANARID[3..0]
PDV	0001B
FVT	0010B
SIT	0011B
SIT-R	0100B
SVT	0101B

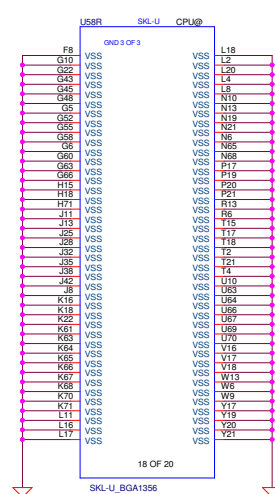
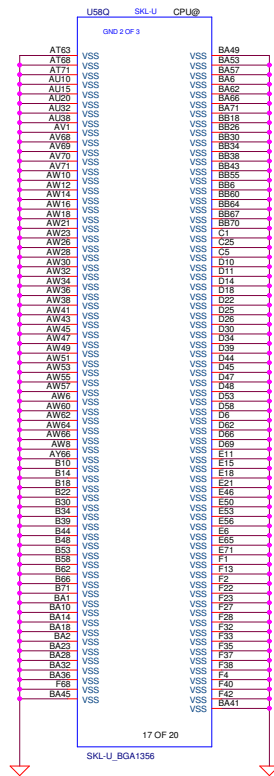
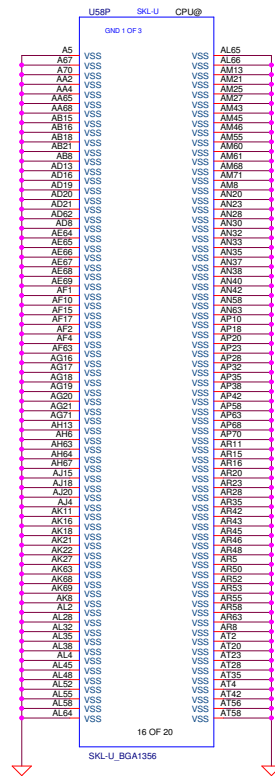
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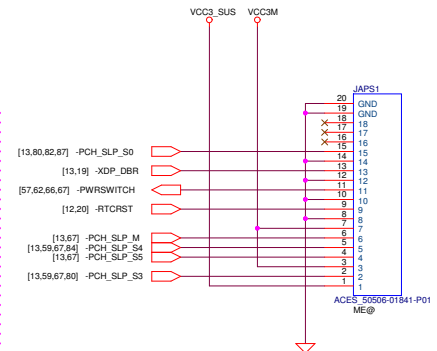


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APS/PETS Interface



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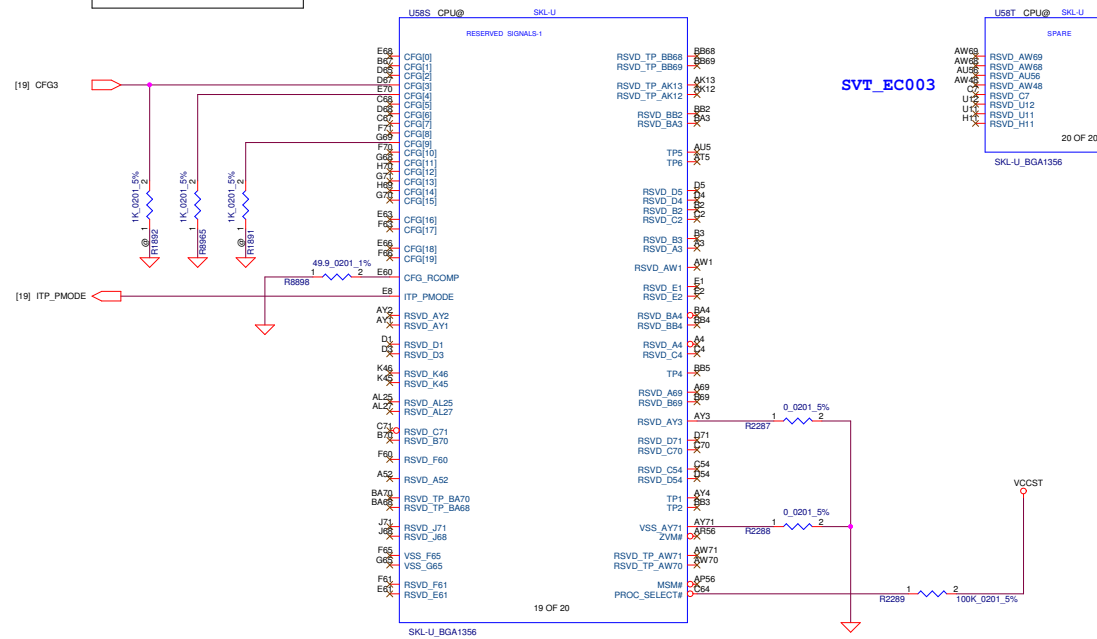
TABLE

CFG0 : Stall Reset Sequence
after PCU PLL Lock until deasserted
1 : No Stall
0 : Stall

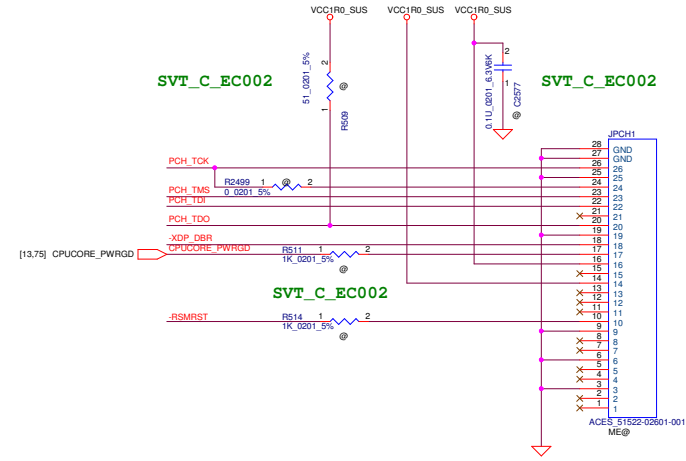
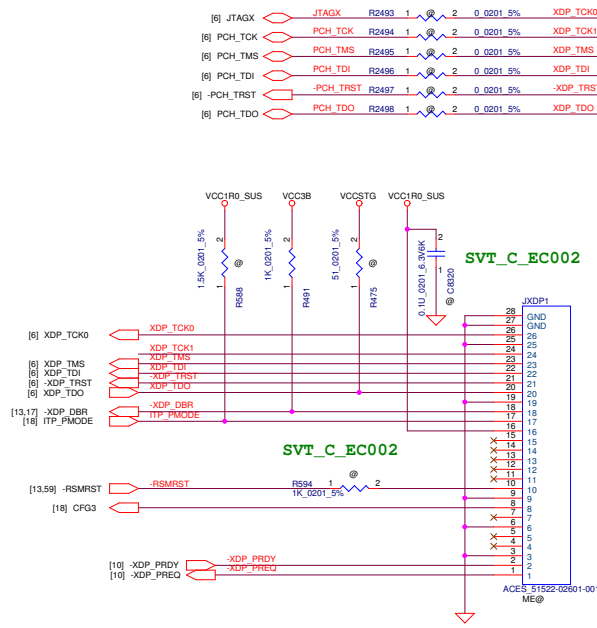
CFG3 : MSR Privacy Bit Feature
1 : MSR (C80h) bit[0] set t i g
0 : MSR (C80h) bit[0] overridden

CFG4 : eDP Enable
1 : Disabled
0 : Enabled

CFG9 : SVID Bus Communicat i on
1 : Enabled
0 : Disabled



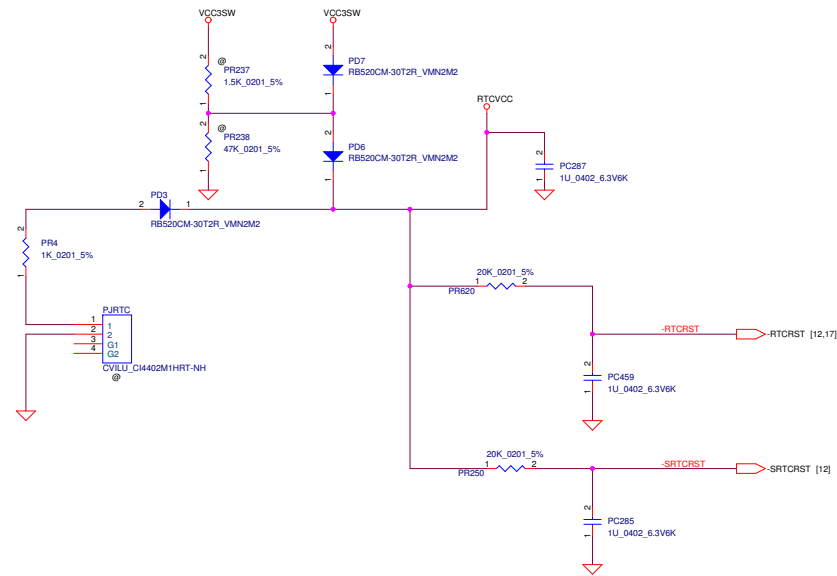
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TABLE

	Individual Port	Merged Port	DCI 2.0 w/o Connector
R2	ASM	ASM	ASM
R471	ASM	NO_ASM	NO_ASM
R541	ASM	NO_ASM	NO_ASM
R515	ASM	NO_ASM	NO_ASM
R530	ASM	NO_ASM	NO_ASM
R475	ASM	ASM	ASM
J8	ASM	ASM	NO_ASM
C8320	ASM	ASM	NO_ASM
R491	ASM	ASM	ASM
R588	ASM	ASM	NO_ASM
R594	ASM	ASM	NO_ASM
R2499	NO_ASM	NO_ASM	NO_ASM
R509	ASM	NO_ASM	NO_ASM
J9	ASM	ASM	NO_ASM
C2577	ASM	ASM	NO_ASM
R511	ASM	ASM	NO_ASM
R514	ASM	ASM	NO_ASM
R2493	NO_ASM	ASM	ASM
R2494	NO_ASM	ASM	NO_ASM
R2495	NO_ASM	ASM	ASM
R2496	NO_ASM	ASM	ASM
R2497	NO_ASM	ASM	ASM
R2498	NO_ASM	ASM	ASM

↑
LOGIC



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- [4] M_A_DQ[63:0]
[4] -M_A_DQS[7:0]
[4] M_A_DQS[7:0]
[4] M_A_A[16:0]

- [4] M_A_CKE0
[4] M_A_BG1
[4] M_A_BG0
[4] M_A_DDRCLK0_933M
[4] -M_A_DDRCLK0_933M
[4] M_A_PARITY
[4] M_A_BS1
[4] -M_A_CS0
[4] M_A_ODT0
[4] -M_A_CS1
[4] M_A_ODT1

- [4] M_A_DQ37
[4] M_A_DQ33
[4] -M_A_DQ54
[4] M_A_DQ54
[4] M_A_DQ38
[4] M_A_DQ34
[4] M_A_DQ44
[4] M_A_DQ40
[4] M_A_DQ46
[4] M_A_DQ42
[4] M_A_DQ52
[4] M_A_DQ49
[4] -M_A_DQ56
[4] M_A_DQ56
[4] M_A_DQ55
[4] M_A_DQ51
[4] M_A_DQ61
[4] M_A_DQ56
[4] M_A_DQ62
[4] M_A_DQ58

- [62:66] SMB_CLK_3B

VCC1R2A

JDMM1

ME@

VCC1R2A

FOX_ASAB5Y-SKSB0-4H

[4] M_A_VREF_CA_CPU

VCC1R2A

M_A_VREF_CA

C2119

0.022U_0201_10V6K

R2074

24.9_0201_1%

M_A_VREF_CA

M_A_VREF_CA

C2120

2.2U_0402_6.3V6M

M_A_VREF_CA

VCC0R6B

VCC0R5A

C2122

10U_0402_6.3V6M

C2123

10U_0402_6.3V6K

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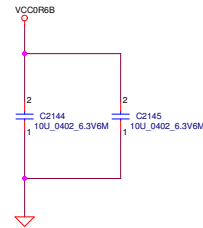
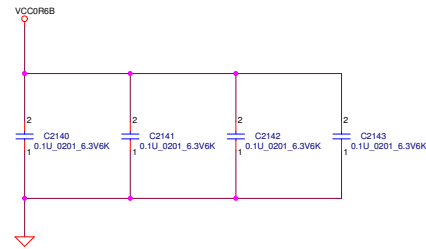
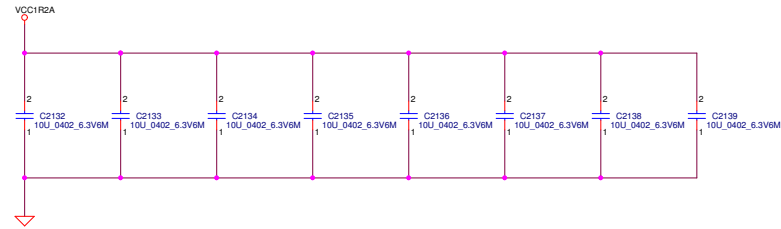
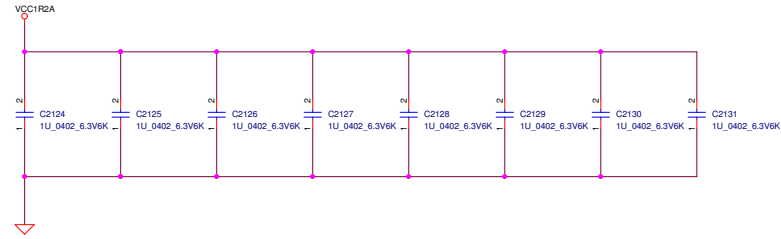
SMB_DATA_3B

SMB_DATA_3B [62:66]

SPD ADDRESS: 50H

SVT_C_EC003

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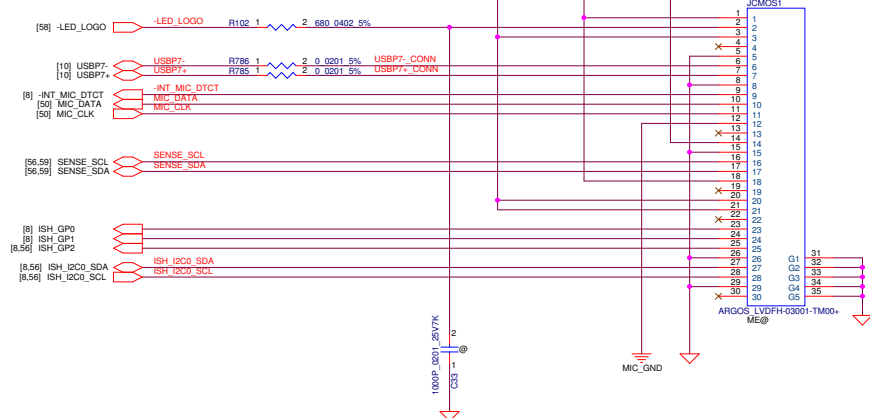
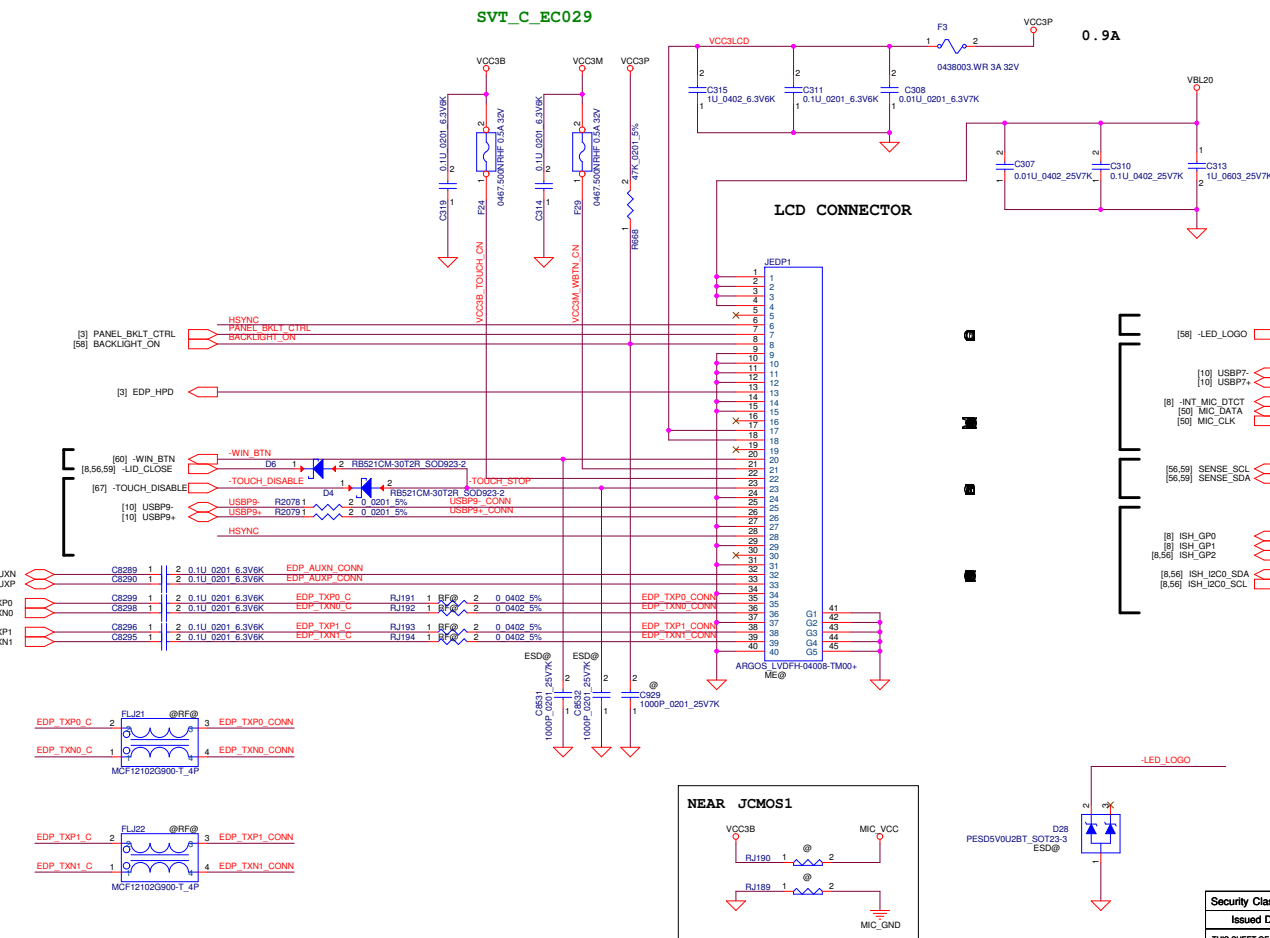
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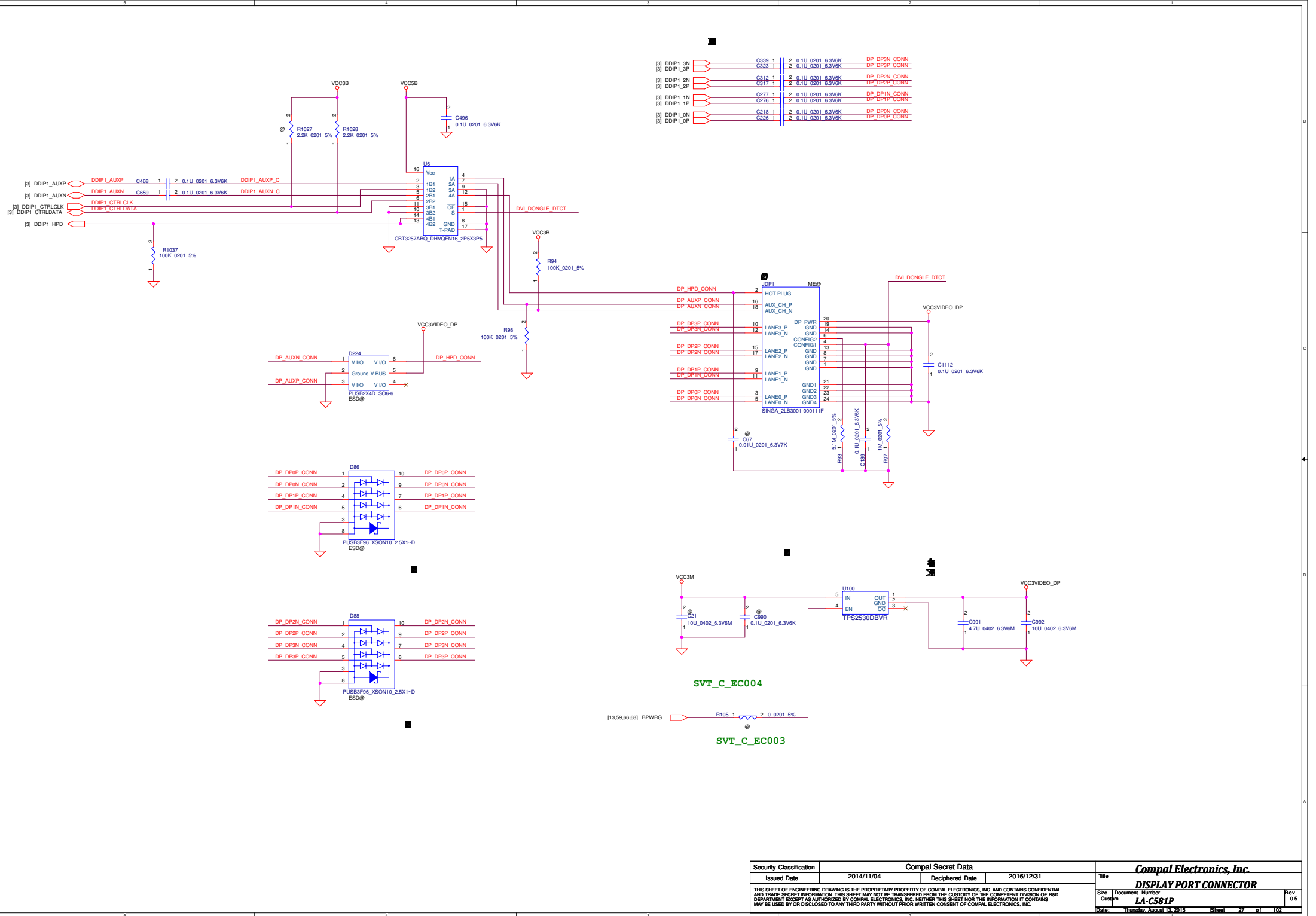
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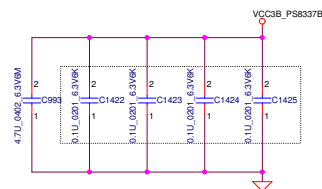
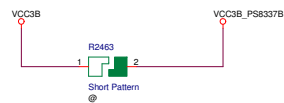


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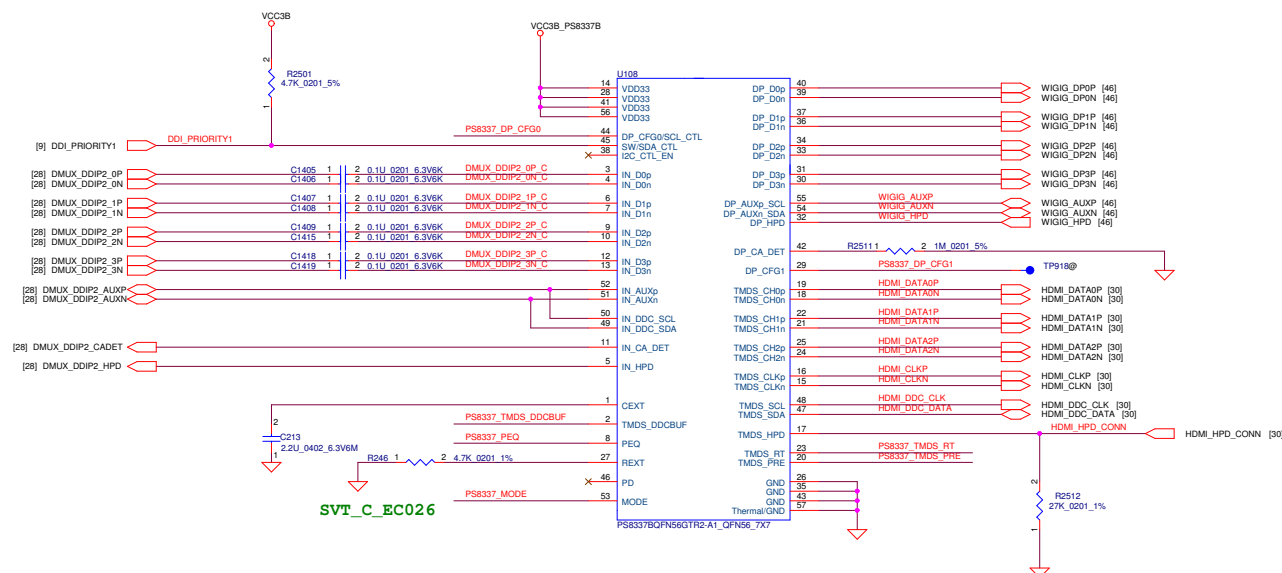


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SW (DDI_PRIORITY1)
L DP Port has higher priority when both ports are plugged H TMDS Port has higher priority when both ports are plugged



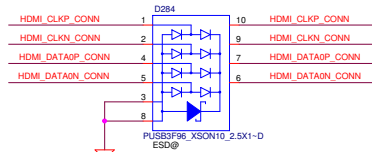
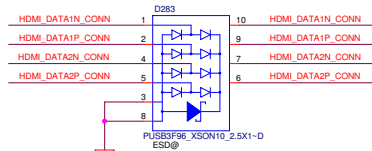
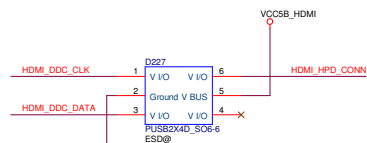
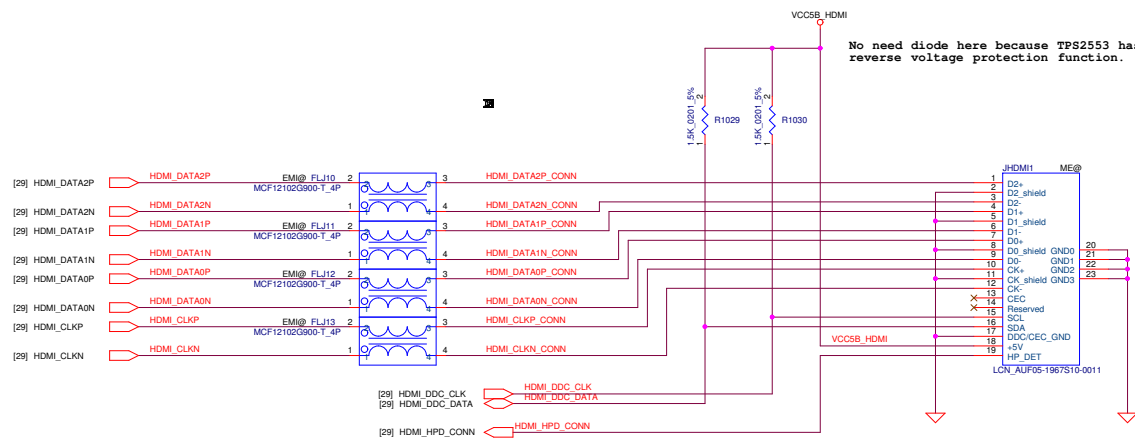
TMD5 DDCBUF (INT PD)	R1876	R1898	
DDC Active Buffer	ASM	NO_ASM	
DDC Pass Through w/ PU	ASM	ASM	
DDC Pass Through w/o PU	NO_ASM	NO_ASM	← LOGIC

PEQ (INT PD)	R1875	R1897	← LOGIC
HEQ 15dB	ASM	NO_ASM	
LLEQ 5dB	ASM	ASM	
LEQ 12dB	NO_ASM	NO_ASM	

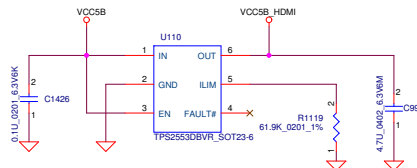
TMS PRE (INT PD)	R1877	R1899
1.5dB	ASM	NO_ASM
3.0dB	ASM	ASM
0dB	NO_ASM	NO_ASM

MODE (INT PD)	R146	R147
Auto HDMI ID disable	ASM	NO_ASM
Auto HDMI ID enable	ASM	ASM
Control HDMI ID disable	NO_ASM	NO_ASM

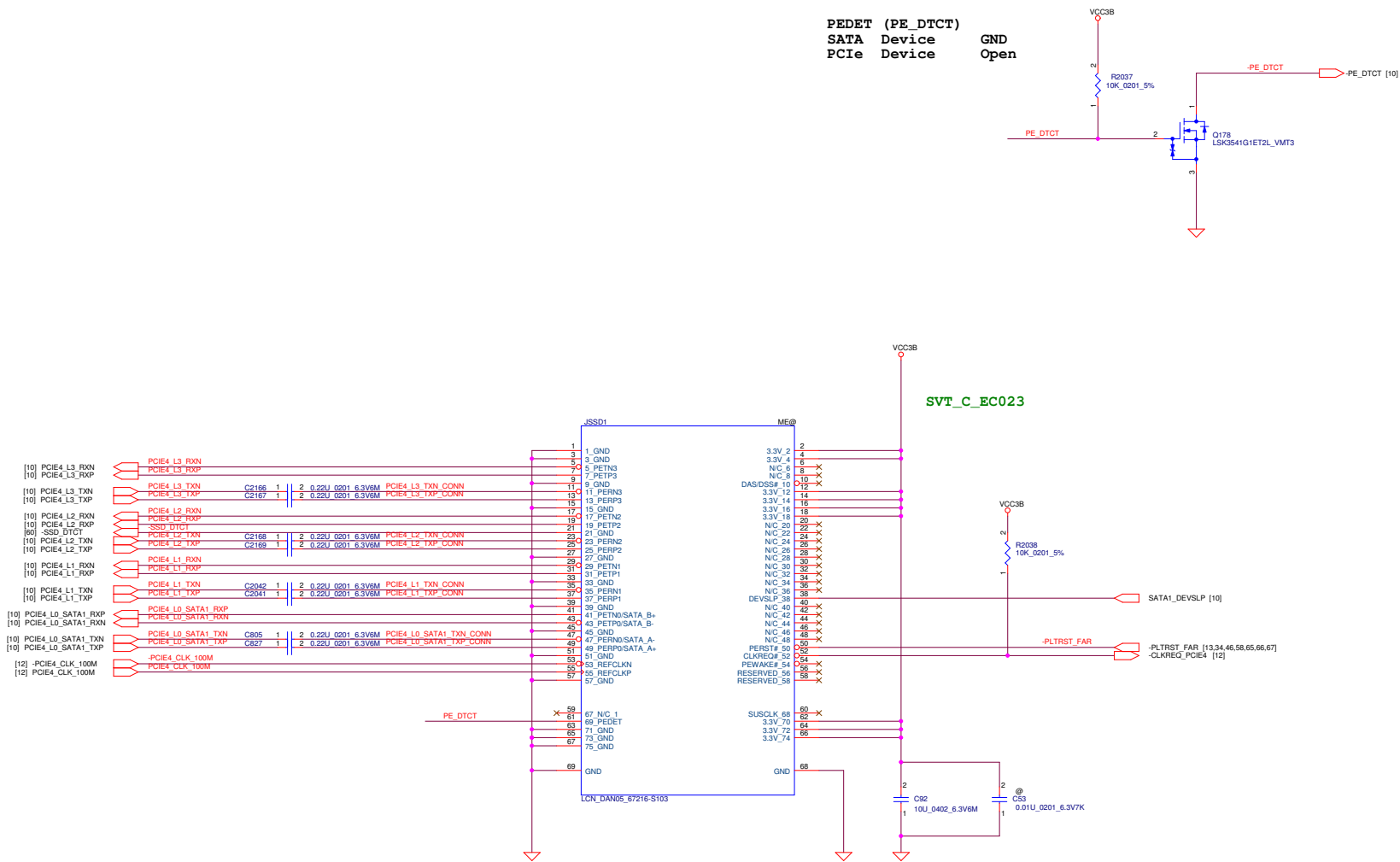
TMDS RT (INT PD)	R2509
OD w/ termination	ASM
OD	NO_ASM



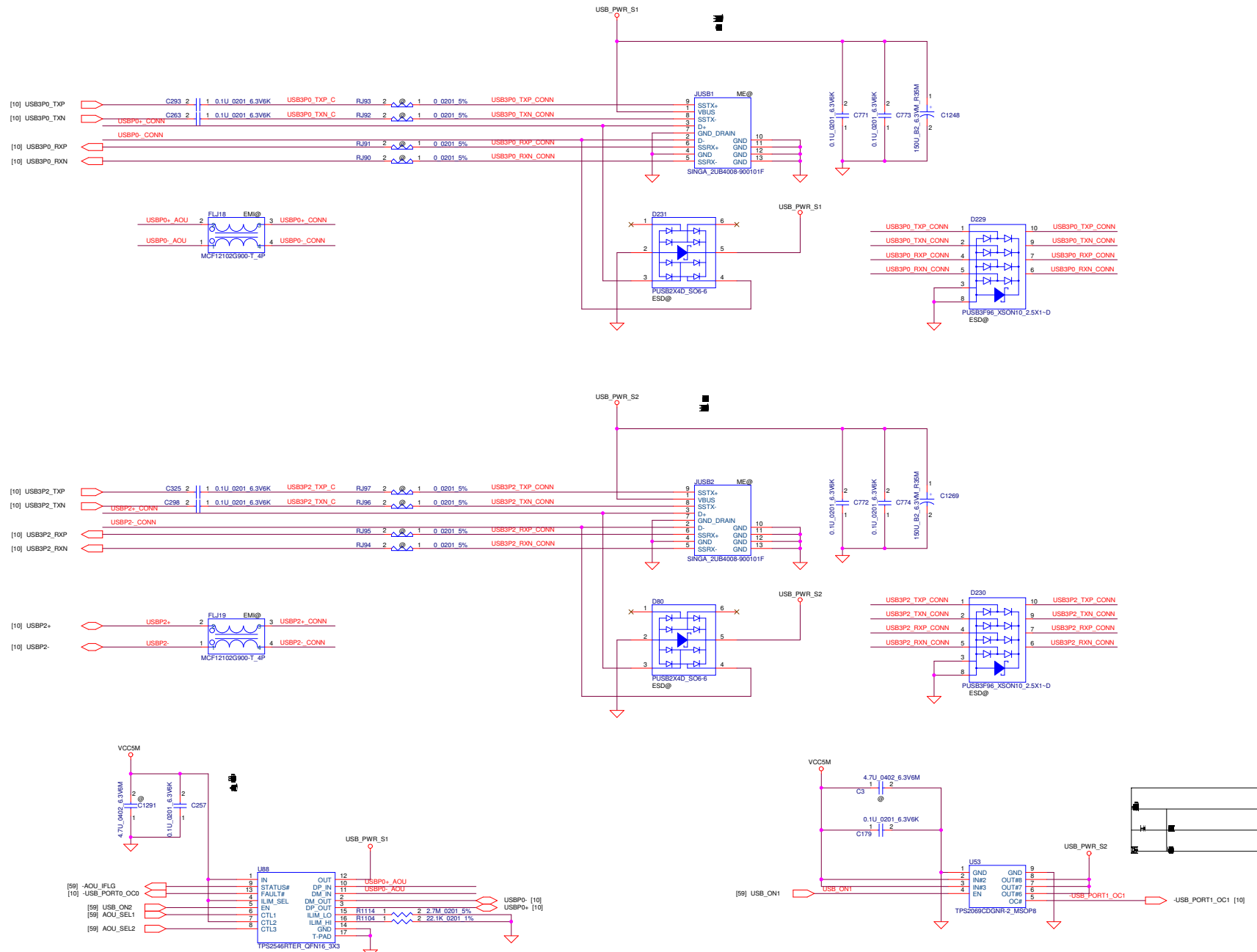
Current Limit Target : 400mA
 Requirement : 300mA
 HDMI Spec : 50mA - 500mA



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				Custom	LA-C581P
				Date	Thursday, August 13, 2015
				Sheet	43 of 102
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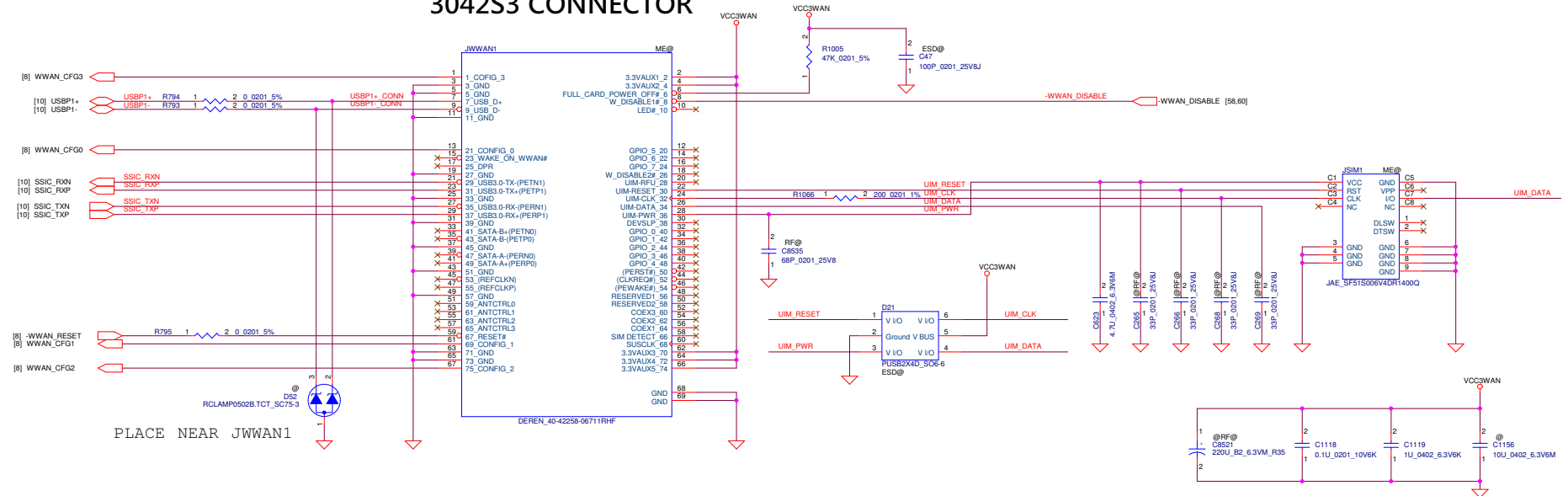
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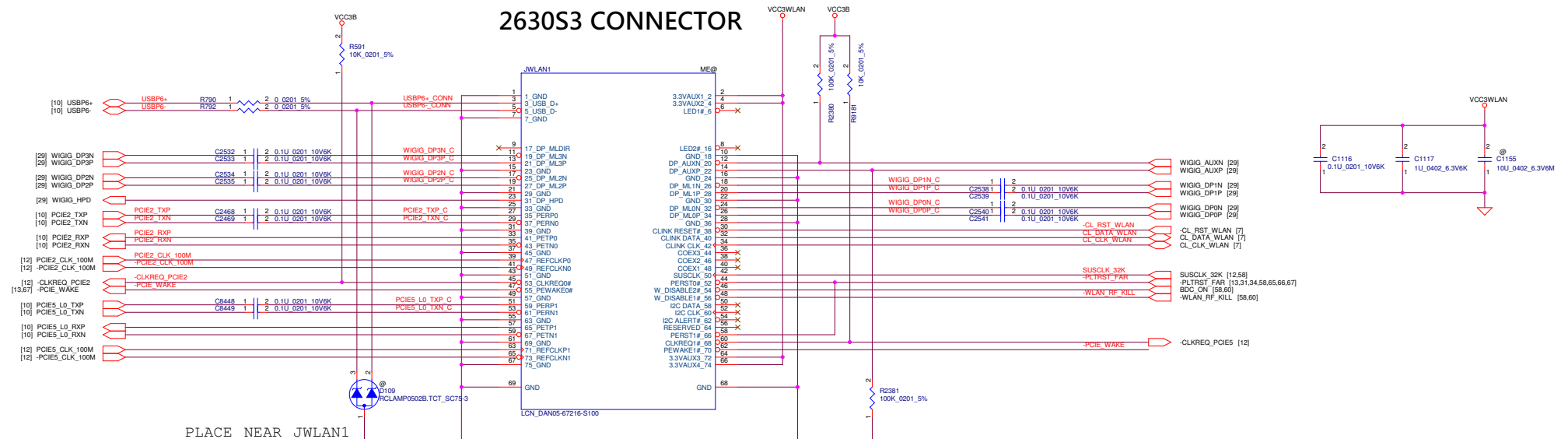
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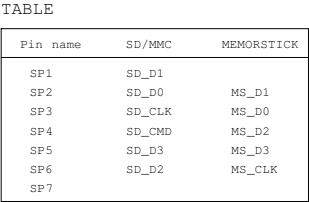
TYPE-B M.2 CARD FOR WWAN

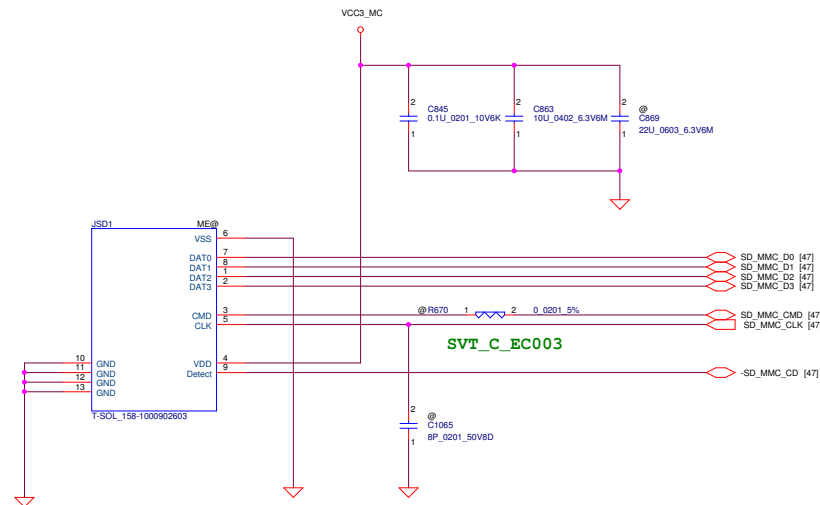


TYPE-A M.2 CARD FOR WLAN / Bluetooth / WiGig

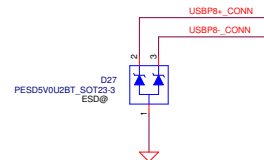
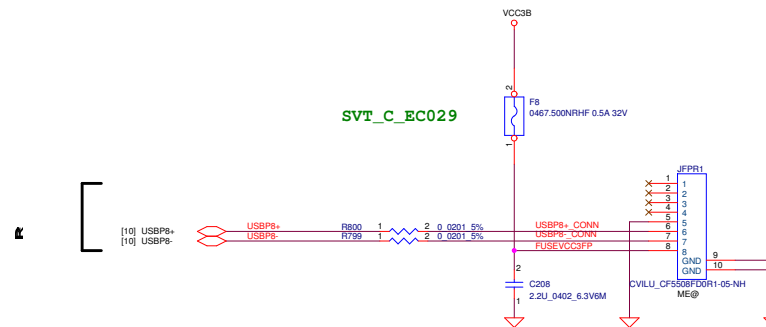
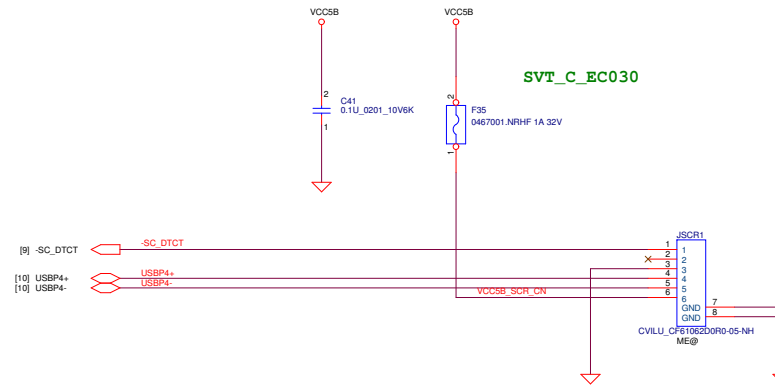


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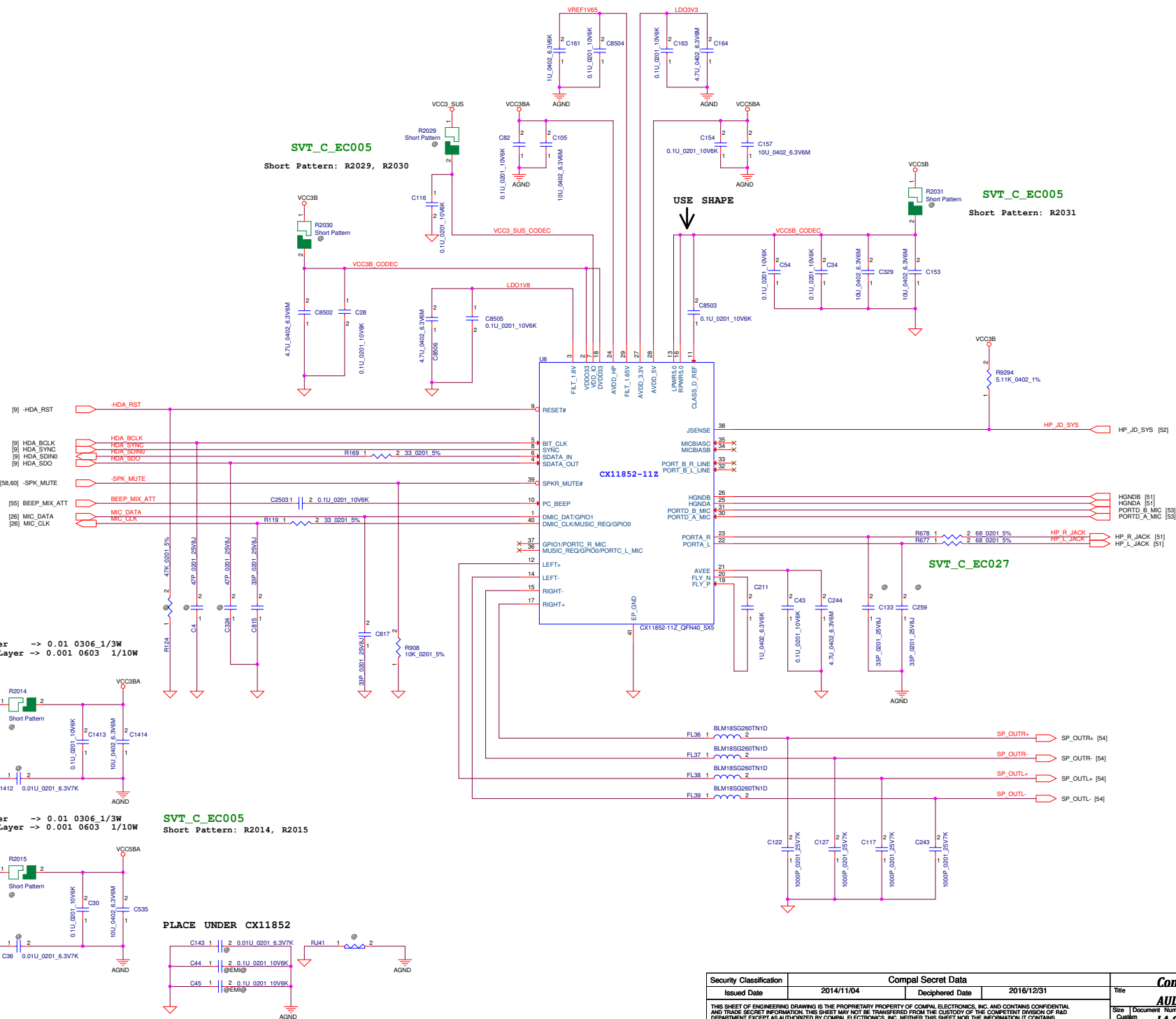




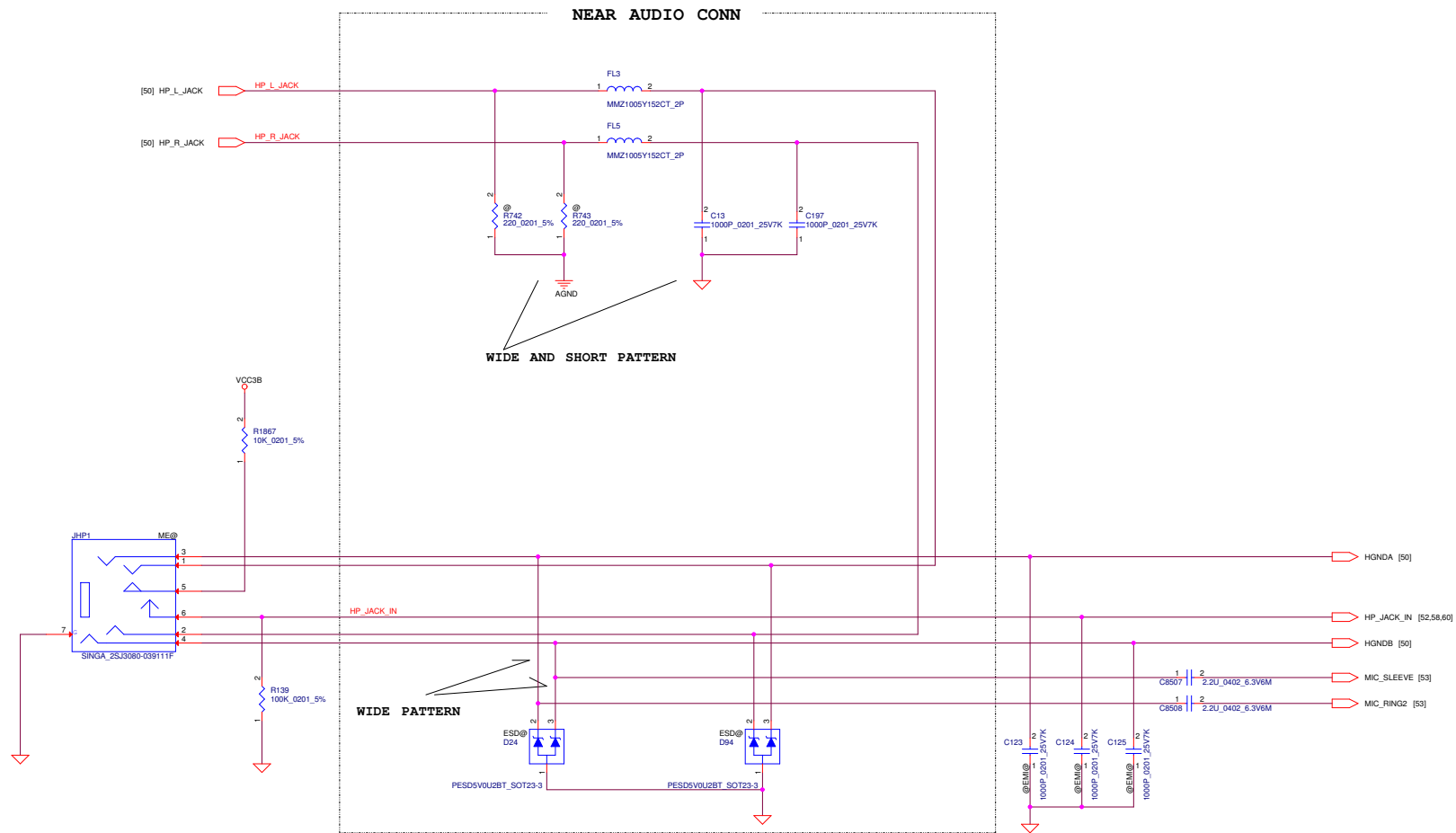
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				Date:	Thursday, August 13, 2015
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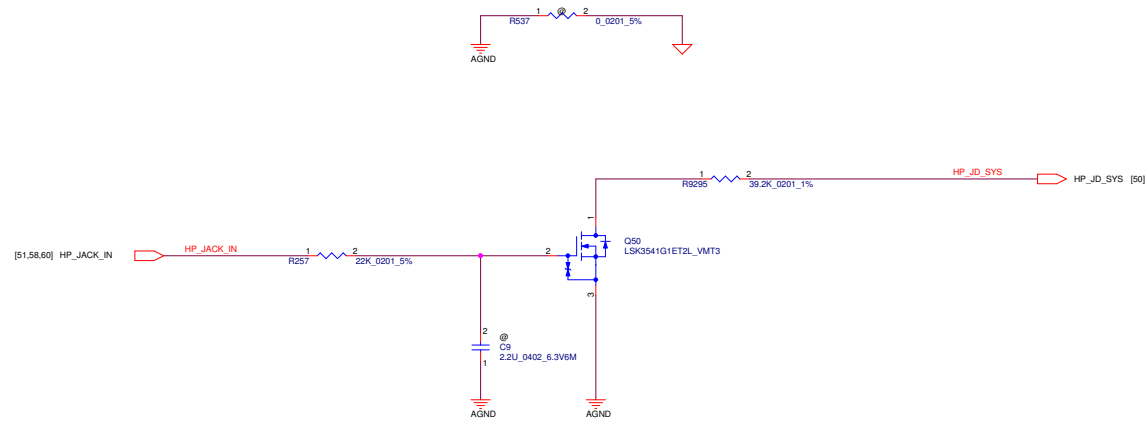
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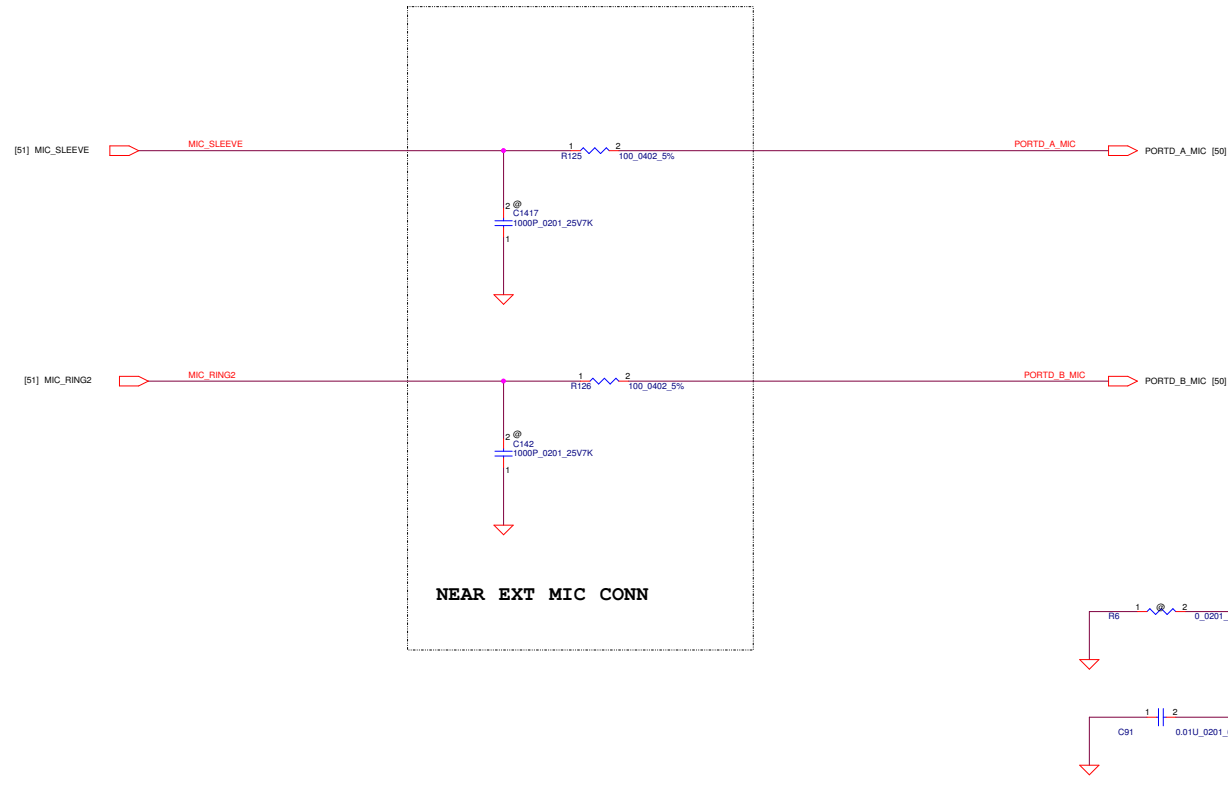
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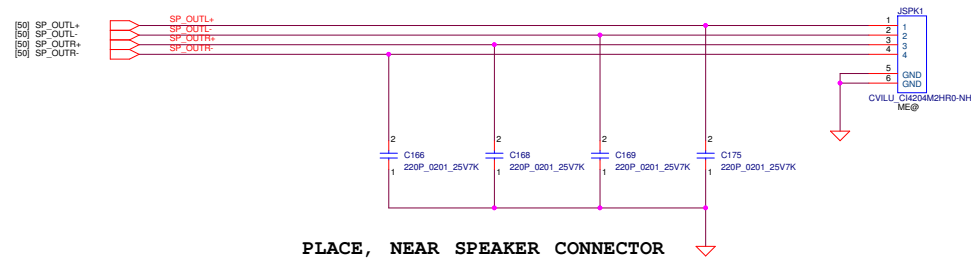
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				Document Number	0.5
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				Date	Thursday, August 13, 2015
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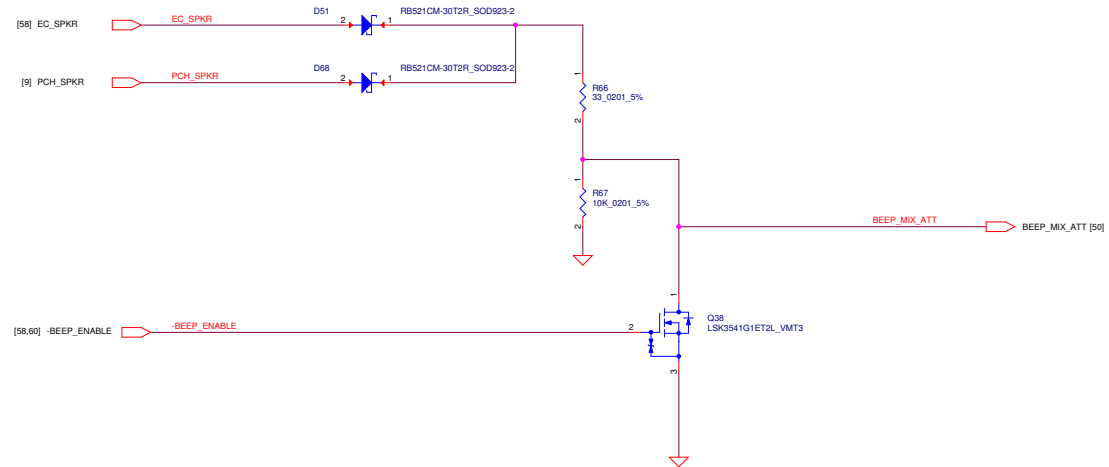
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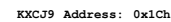
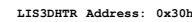
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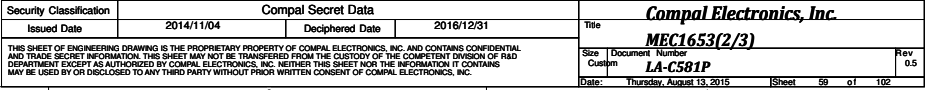
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H	I2C Mode
L	SPI Mode

ACC2_SA0	Address Selection
H	32h (W) & 33h (R)
L	30h (W) & 31h (R)

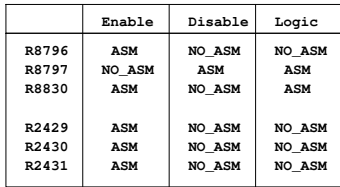


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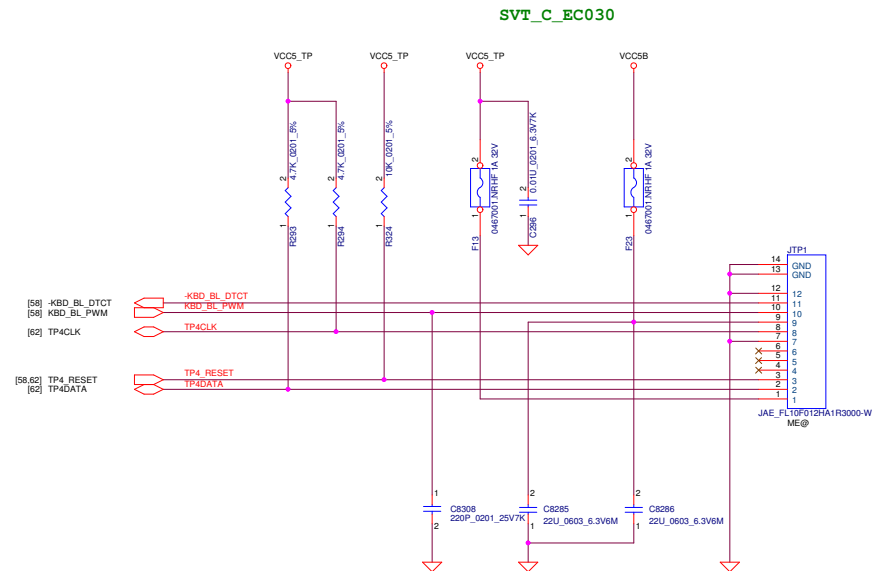
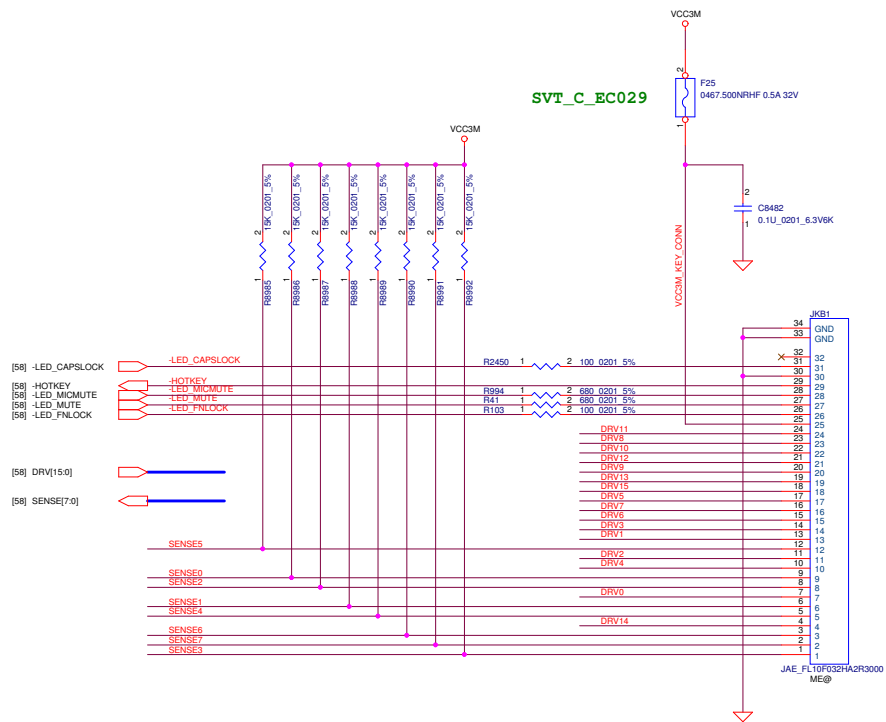




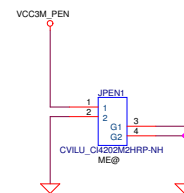
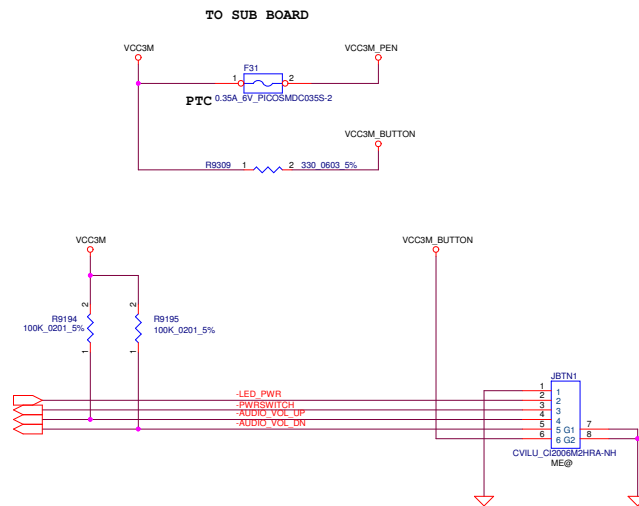
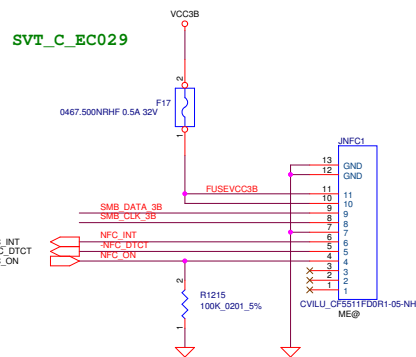
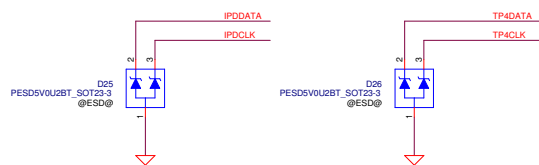
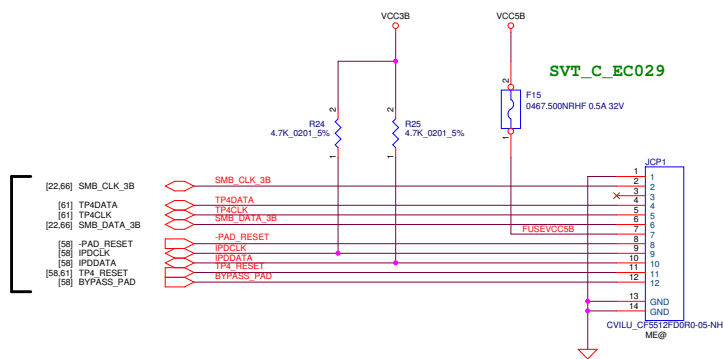
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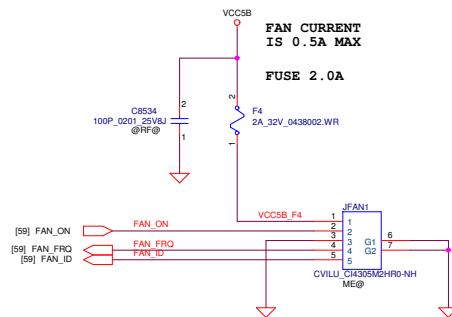
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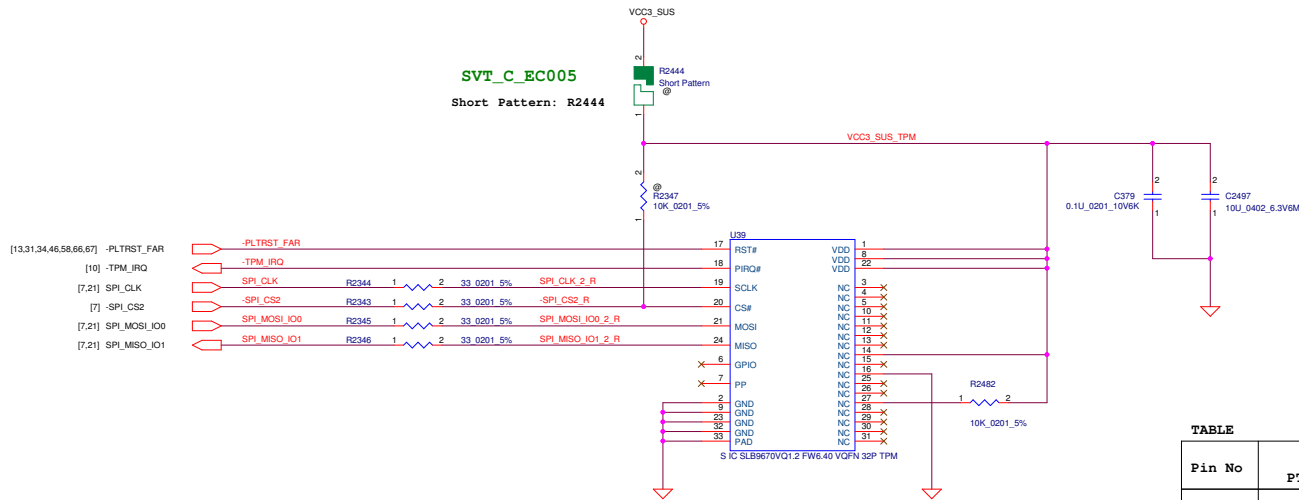
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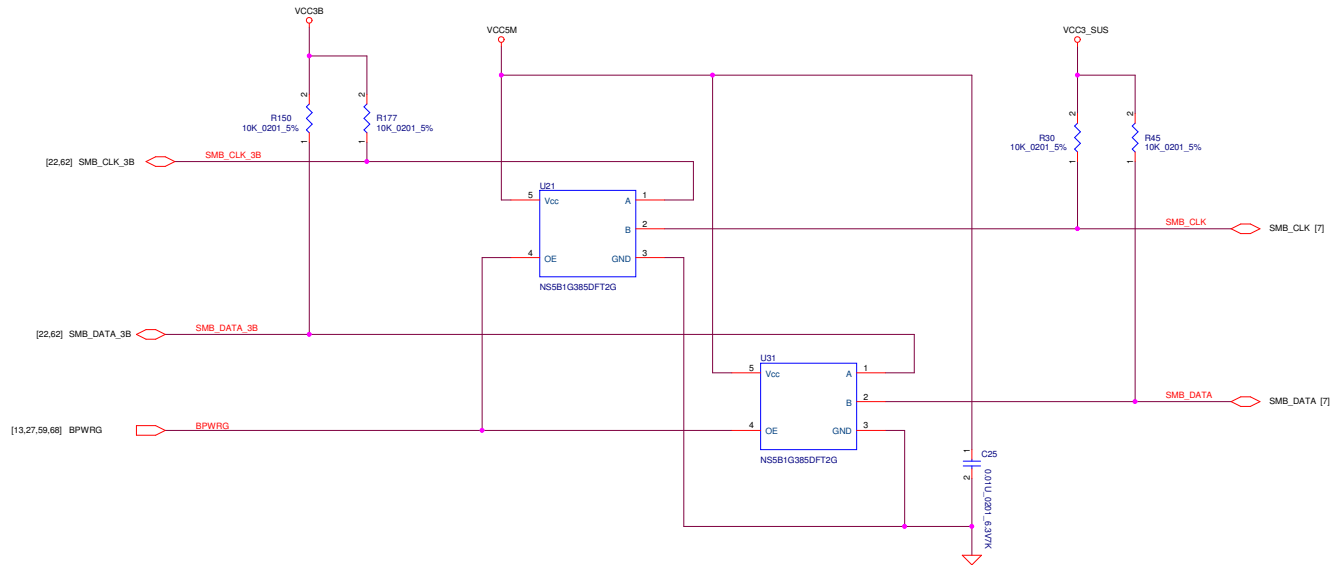
-Change FW version of Infineon TPM to 6.40
-Change Nuvoton parts number to NPCT650LB0YX

TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ1.2 FW 6.40	Nuvoton NPCT650LB0YX
1	VDD	VDD	VSB
2	GND	GND	NC
3	GPIO	NC	GPX/GPIO2
4	GPIO	NC	PP
5	NC	NC	TEST
6	VNC/GPIO	GPIO	GPIO3
7	GPIO/VDD	PP	NC
8	VDD	VDD	VDD
9	GND	GND	GND
10	VNC	NC	NC
11	NC	NC	NC
12	NC	NC	Reserved
13	VNC/GPIO	NC	GPIO4
14	VDD	NC	VDD
15	NC	NC	DNC
16	GND	NC	GND
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#
19	SPI_CLK	SCLK	SCLK
20	SPI_CS#	CS#	SCS#
21	MOSI	MOSI	MOSI
22	VDD	VDD	VDD
23	GND	GND	GND
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	(SERIRQ)
28	NC	NC	DNC
29	VNC/ GPIO	NC	GPIO0
30	VNC/ GPIO	NC	GPIO1
31	VNC	NC	NC
32	GND	GND	GND

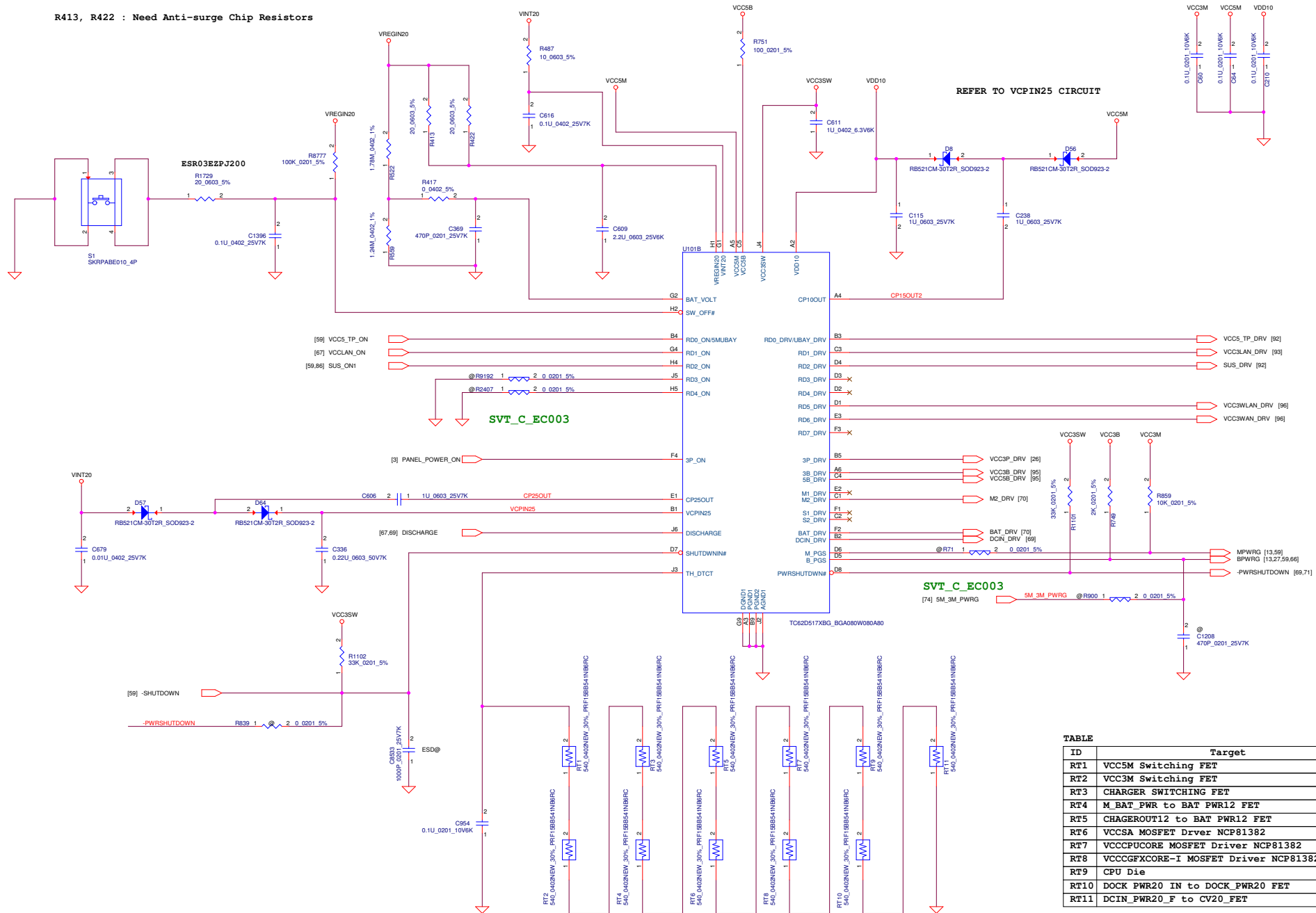
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SVT_EC004



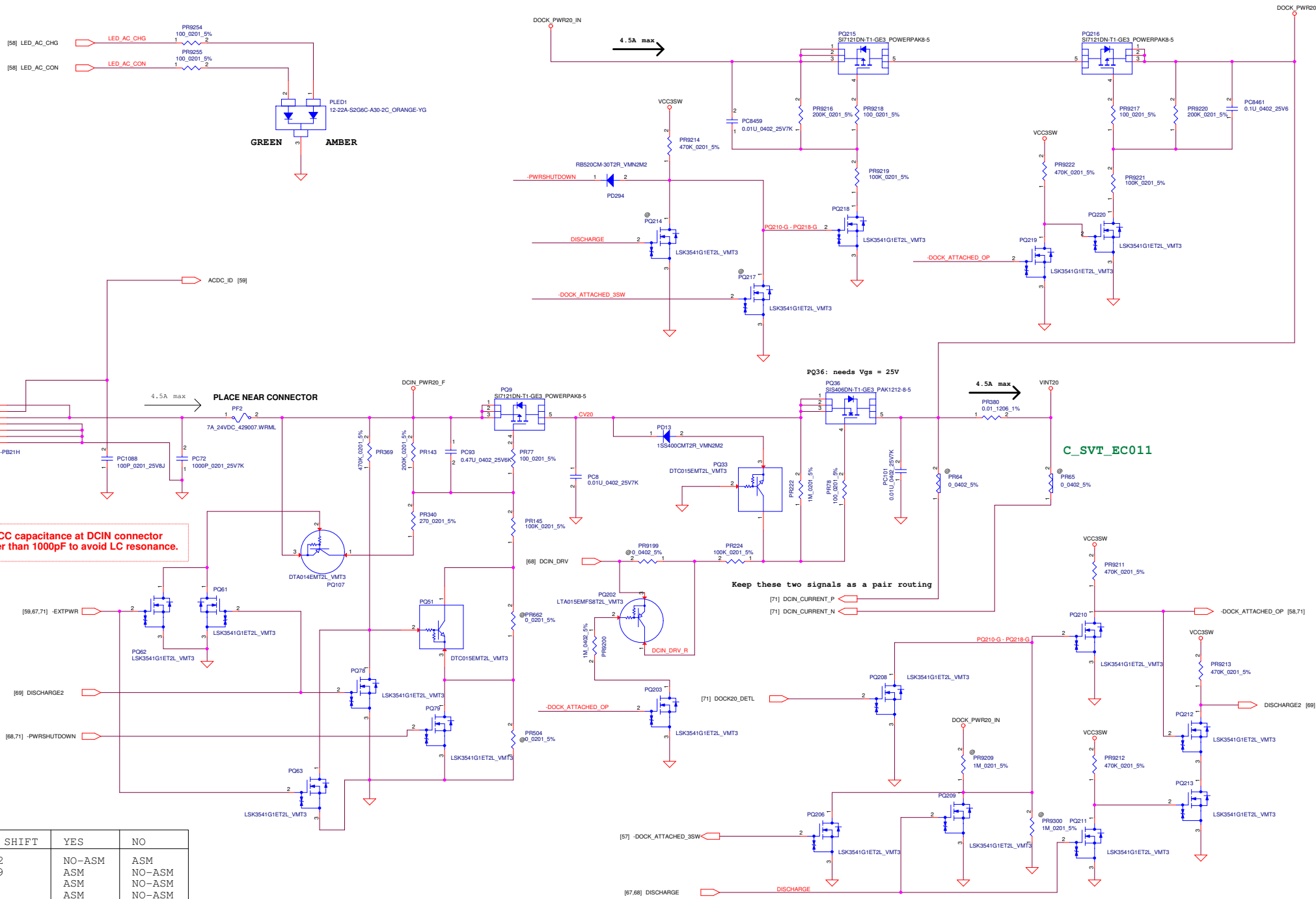
WWW.AliSaler.Com

R413, R422 : Need Anti-surge Chip Resistors



ID	Target
RT1	VCC5M Switching FET
RT2	VCC3M Switching FET
RT3	CHARGER SWITCHING FET
RT4	M_BAT_PWR to BAT_PWR12 FET
RT5	CHAGEROUT12 to BAT_PWR12 FET
RT6	VCCSA MOSFET Driver NCP81382
RT7	VCCPCUCORE MOSFET Driver NCP81382
RT8	VCCCGFXCORE-I MOSFET Driver NCP81382
RT9	CPU Die
RT10	DOCK_PWR20 IN to DOCK_PWR20 FET
RT11	DCIN_PWR20 F to CV20_FET

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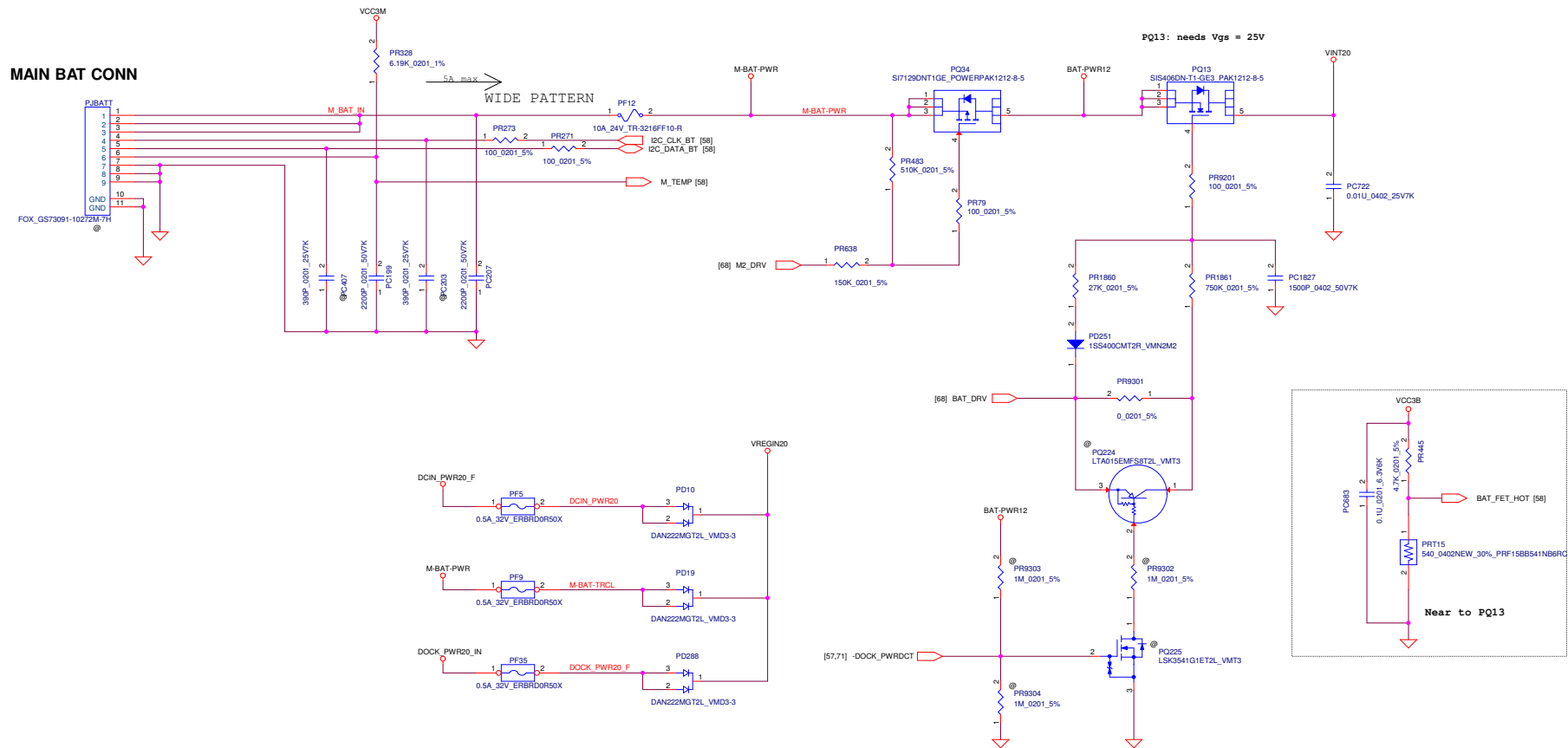
Total MLCC capacitance at DCIN connector is smaller than 1000pF to avoid LC resonance.

TABLE		
PEAK SHIFT	YES	NO
PR662	NO-ASM	ASM
PR369	ASM	NO-ASM
PQ78	ASM	NO-ASM
PQ51	ASM	NO-ASM

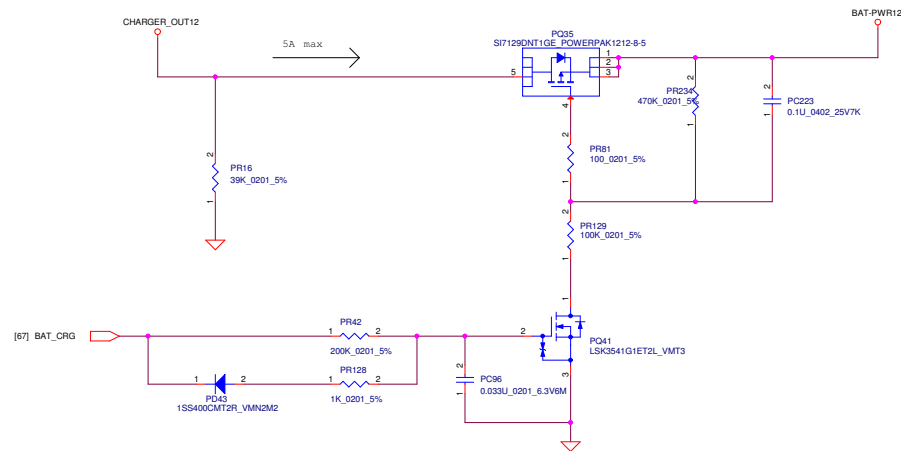
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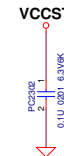
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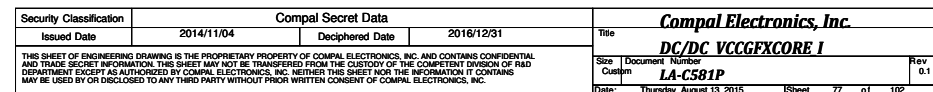
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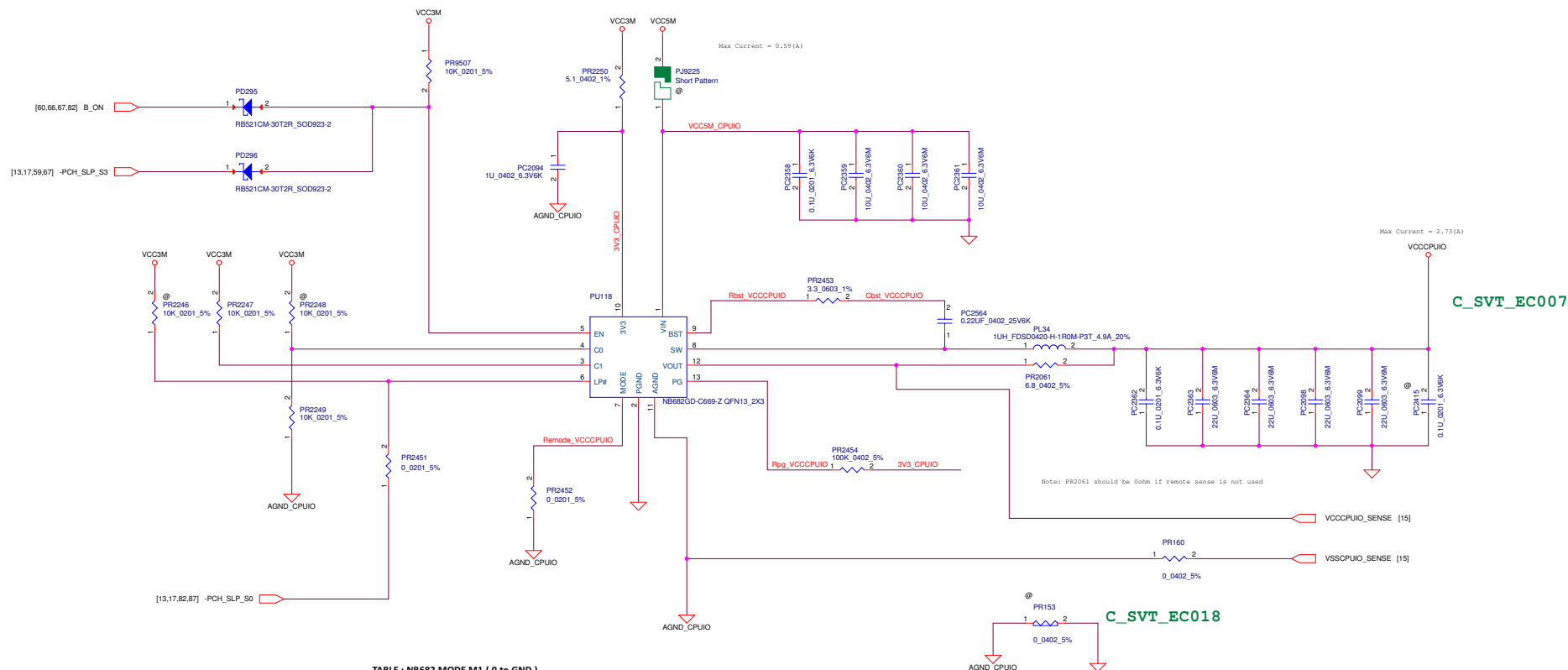


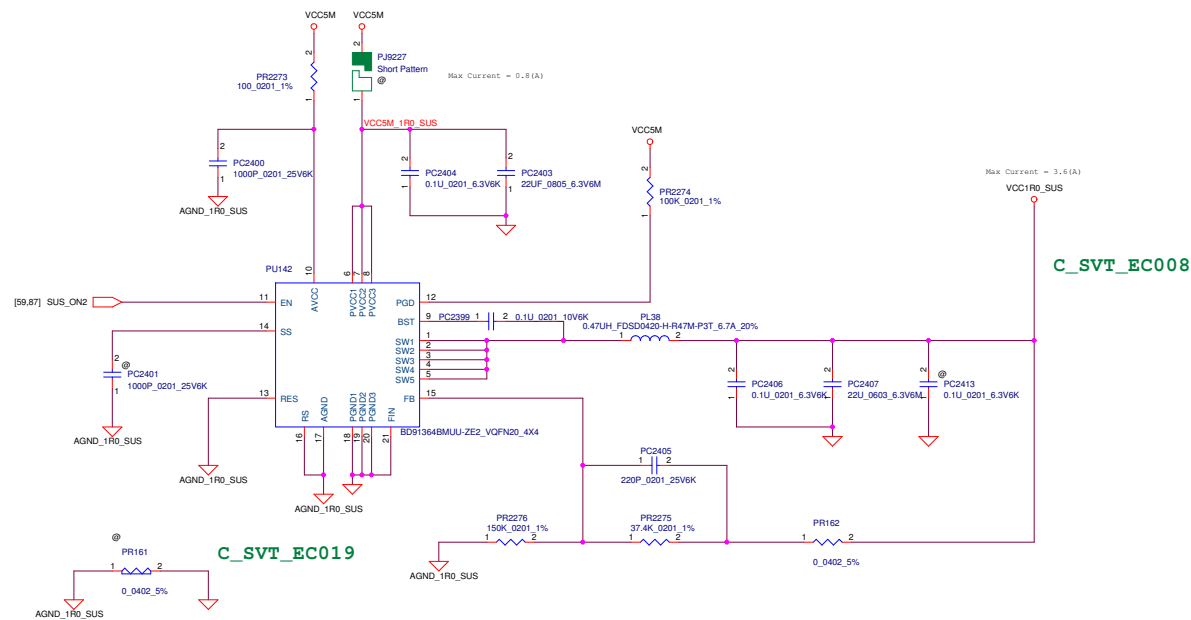
TABLE : NB682 MODE M1 (0 to GND)

LP#	C1	C0	VOUT
0	X	X	0.000V
1	0	0	0.850V
1	0	1	0.875V
1	1	0	0.950V
1	1	1	0.975V

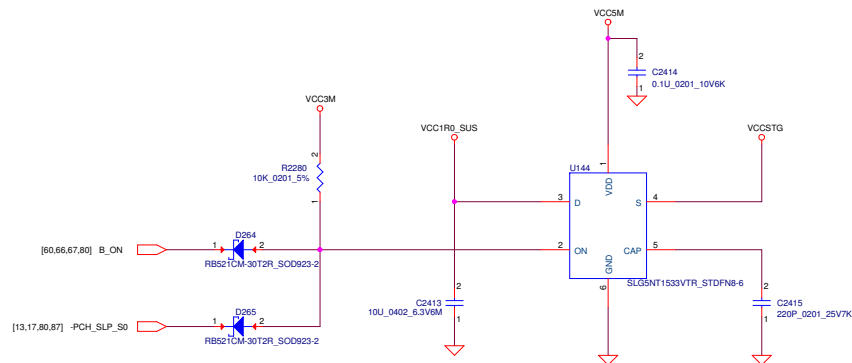
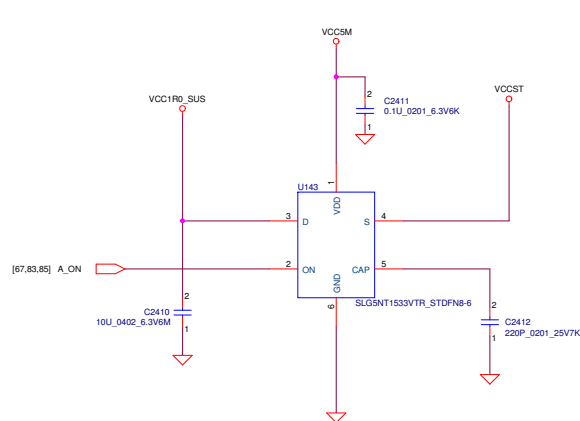
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← LOGIC

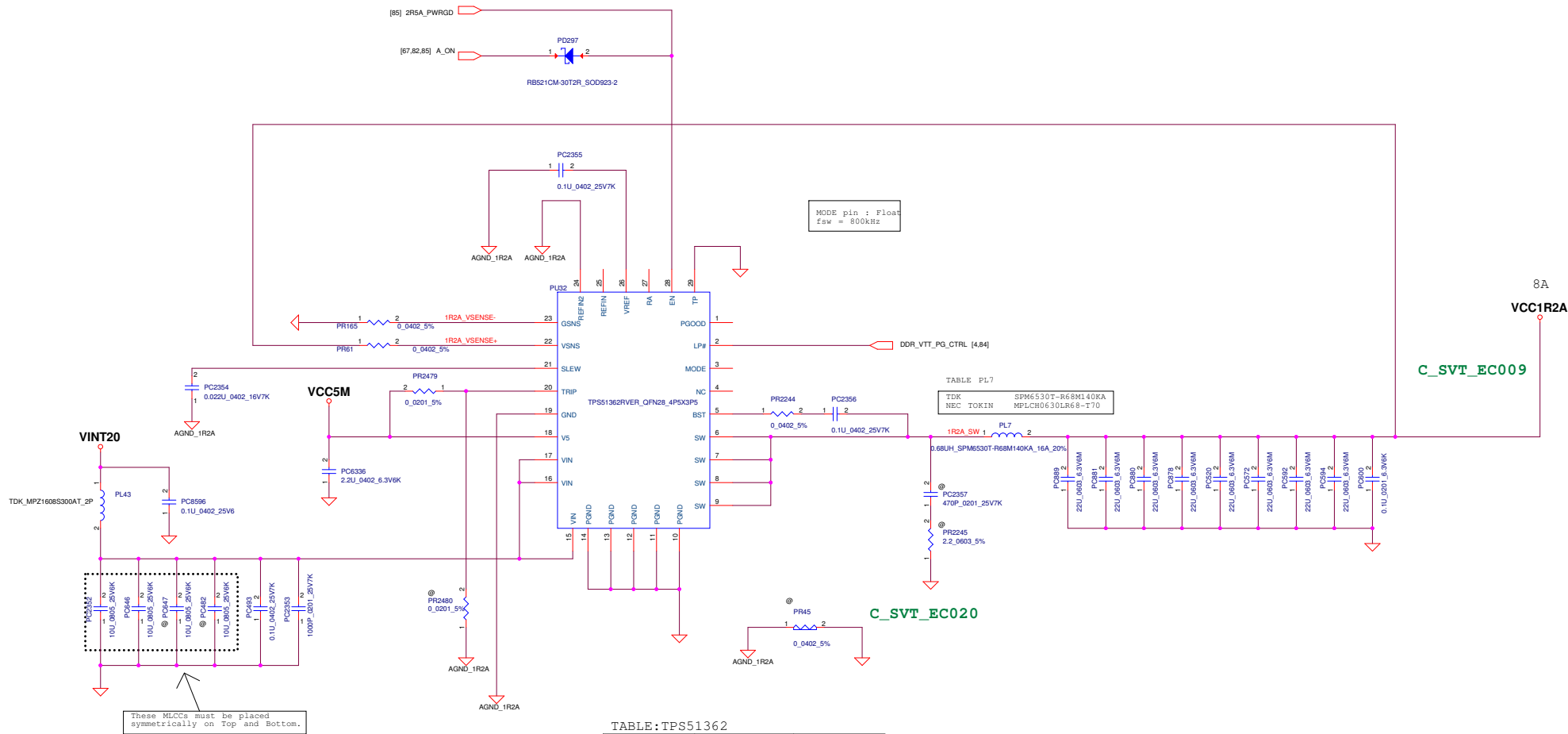
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MODE pin : Float
fsw = 800kHz

TABLE PL7

TDK	SPM6530T-R68M140KA
NEC	TOKIN
	MPLCH0630LR66-T70

TABLE:TPS51362

REFIN	REFIN2	VOUT
GND	GND	1.05V
Float	GND	1.20V
GND	Float	1.50V
Float	Float	1.35V

← LOGIC

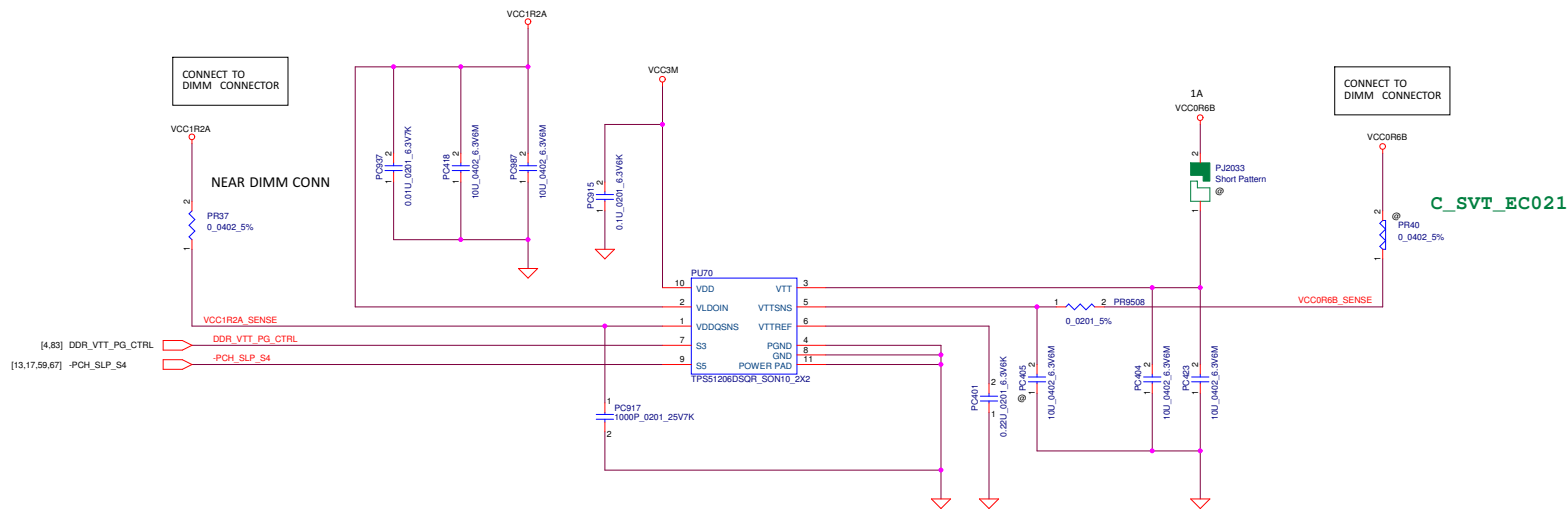
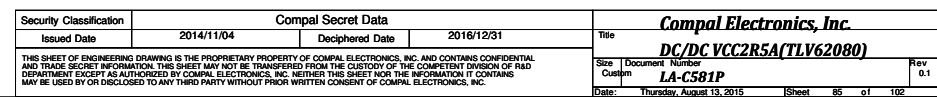
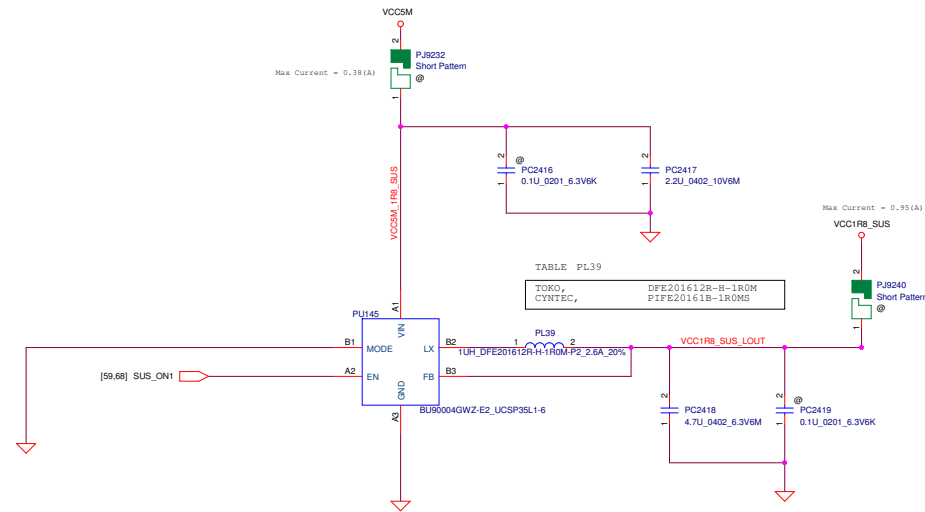


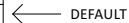
TABLE : TPS51206

S3	S5	VTT	VTTREF
High	High	ON	ON
Low	High	OFF(High-Z)	ON
Low	Low	OFF(Discharge)	OFF(Discharge)





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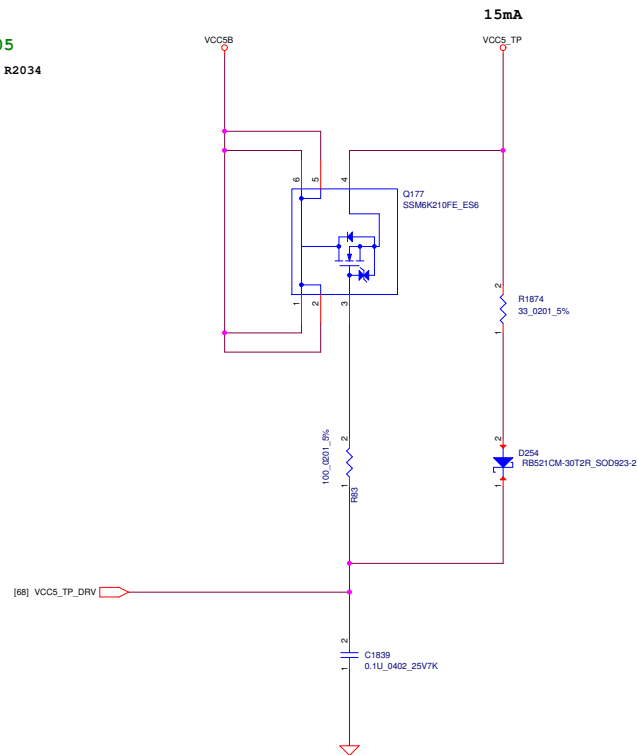
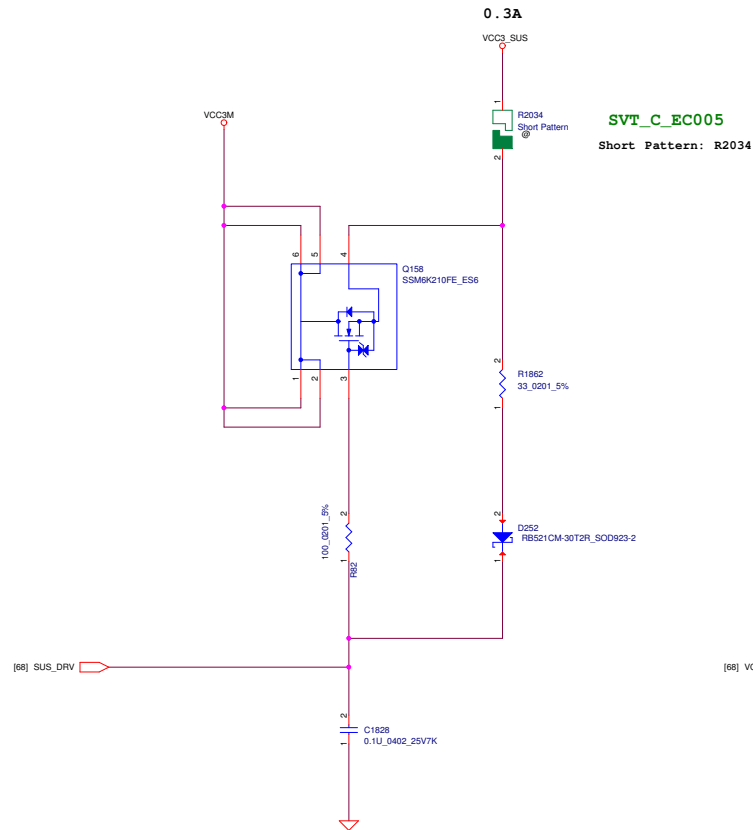
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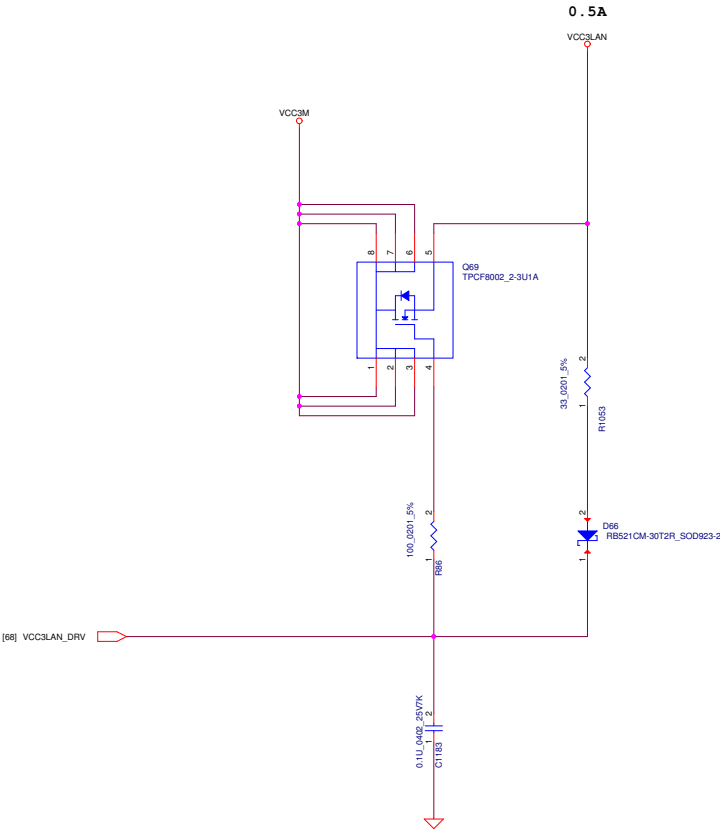
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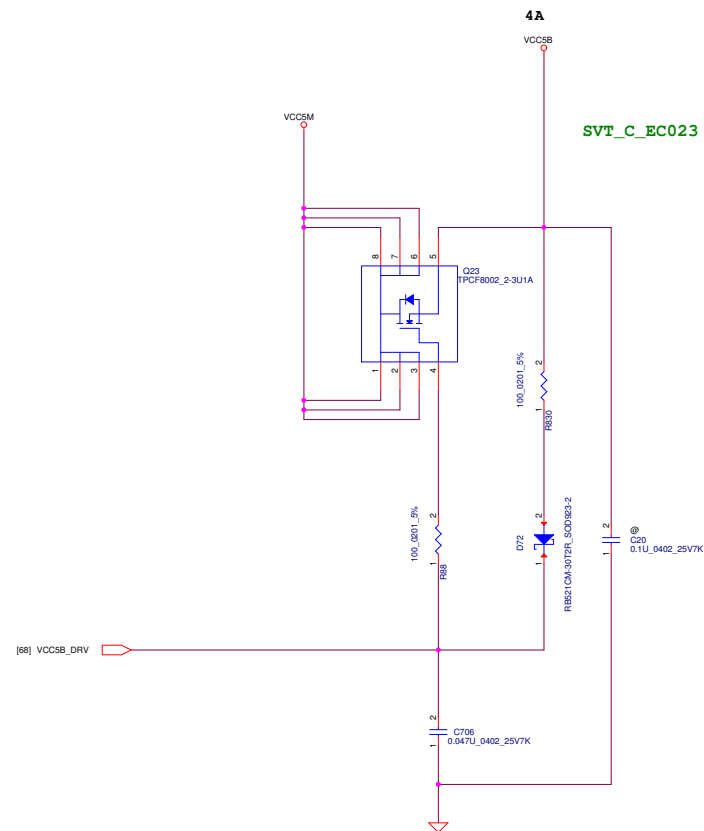
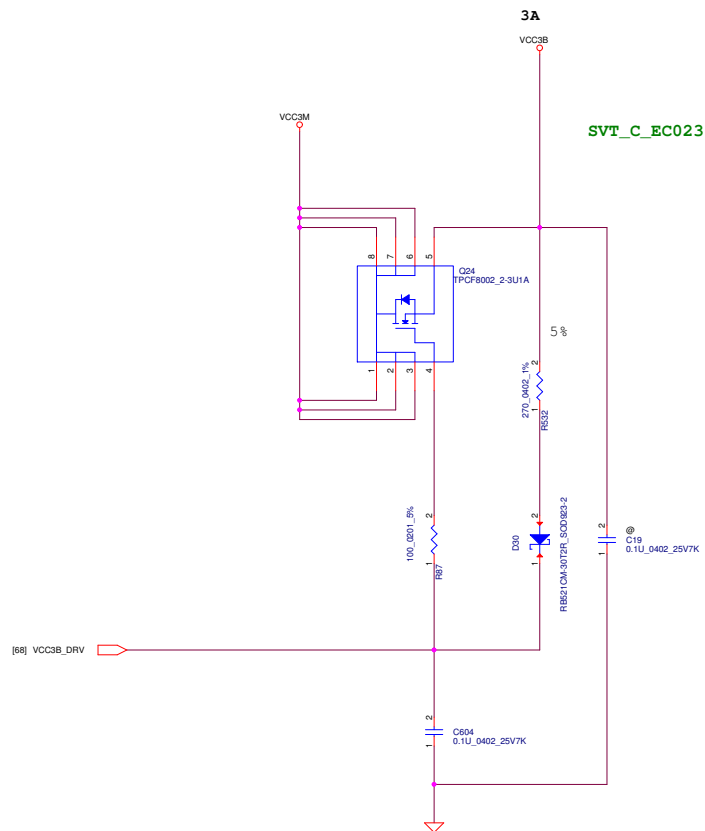
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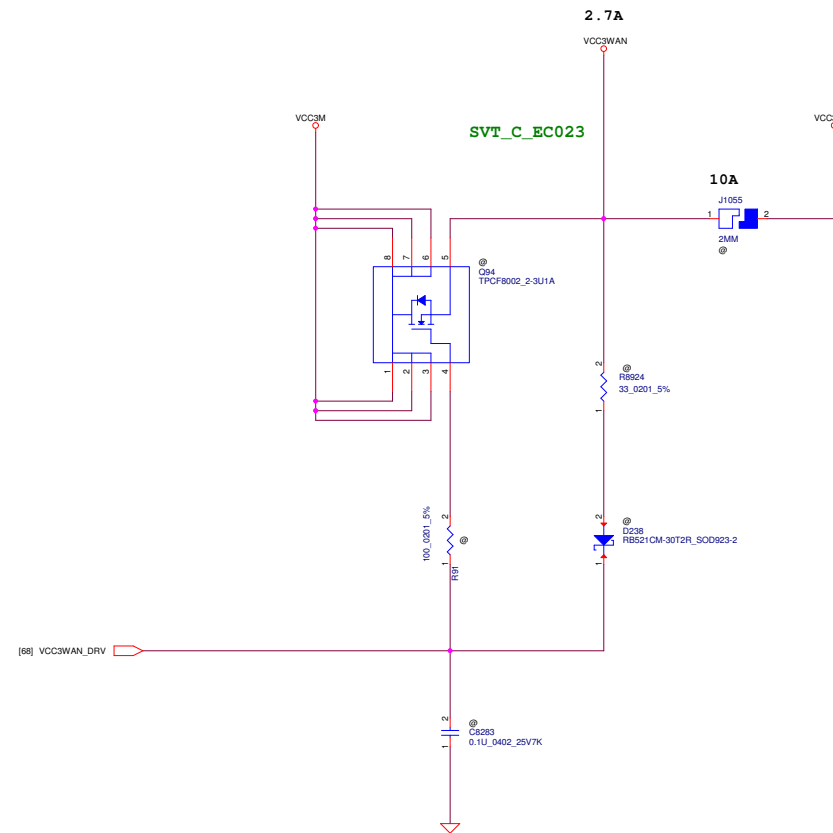
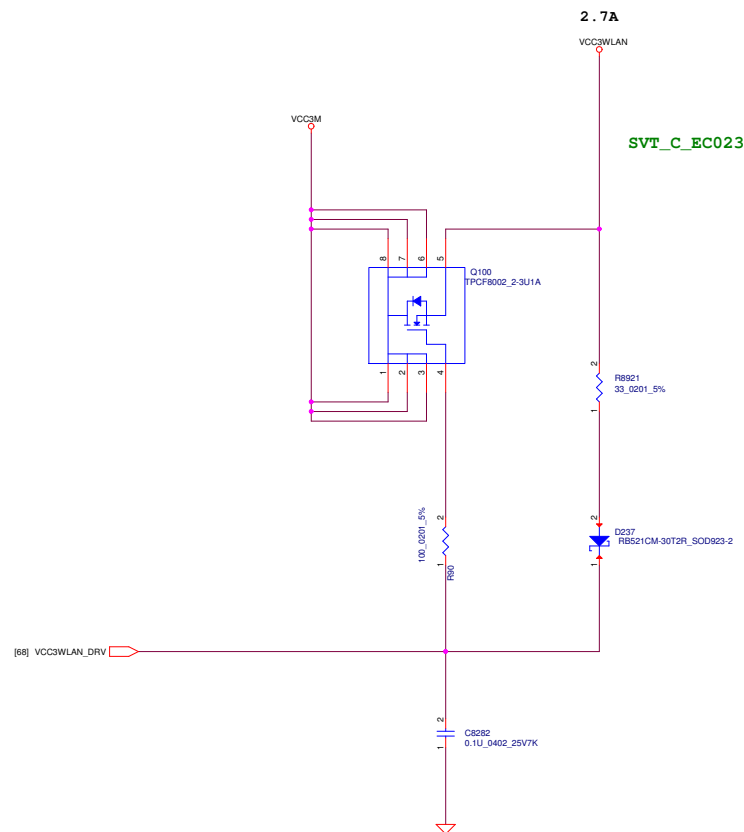
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TABLE

AOAC	YES	NO
R1055	NO-ASM	ASM
Q94	ASM	NO-ASM
R91	ASM	NO-ASM
R8924	ASM	NO-ASM
C8283	ASM	NO-ASM
D238	ASM	NO-ASM

↑
LOGIC

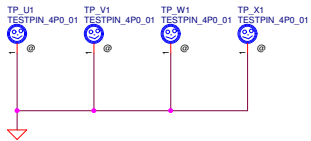
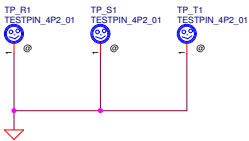
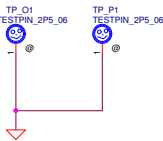
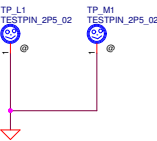
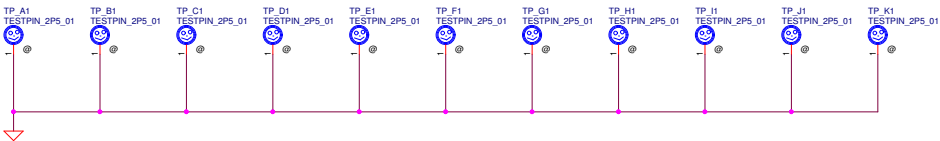
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PTH FOR SCREW HOLE

Value	Hole Dia	Pad Dia		Qty
		TOP	BOTTOM	
TESTPIN_2P5_01	2.5	6	6	11
TESTPIN_2P5_02	2.5	7.4	7.4	2
TESTPIN_2P5_03	2.5	Square	0	1
TESTPIN_2P5_06	2.5	5	5	2
TESTPIN_2P8_01	2.8	0	Square	1
TESTPIN_4P3_01	4.3	6.5	6.5	3
TESTPIN_4P0_01	4.0	6.1	6.1	4



NPTH



FID
Board Area

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